MareNostrum Experimental Exascale Platform

MEEP
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www.meep-project.eu

Francelly K. Cano Ladino (BSC-CNS) francelly.canoladino@bsc.es
(on behalf of the MEEP Project meep-project@bsc.es)

WHAT IS MEEP?

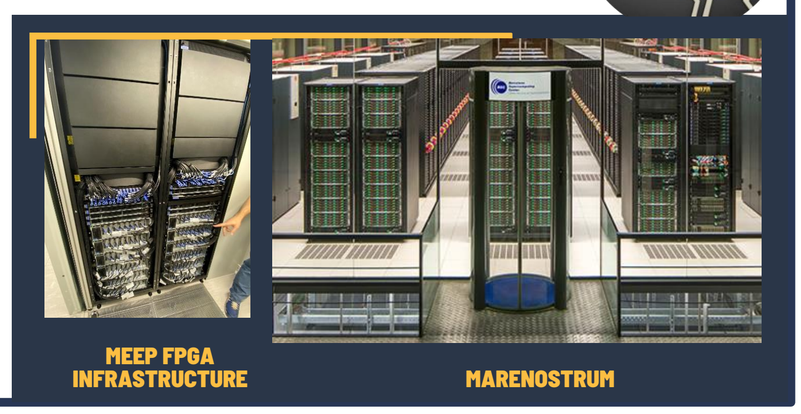
- HW&SW Co-design lab for HPC
- 3 year project (Jan 20 - June 23)
- 10M€ budget
- Based on RISC-V Open Source & European Processors

A digital laboratory that enables SW/HW co-design for pre-silicon validation of hardware IPs and a corresponding software development vehicle.

Motivation:
- End of Moore's Law and power constraints require software/hardware co-design.
- Leverage the technology scaling in mobile chips leads to a chiplet architecture for HPC.
- Chip fabrication increasing in cost => need to pre-silicon validation of designs.
- Hardware platform for software development before the final targeted architecture is available.

Main components of MEEP
- **HW**:
  - Infrastructure: Large scale FPGA-based platform (96 FPGAs in 12 nodes)
  - Catalogue of open-source IPs
    - Example 1: **ACME** (Research accelerator design with a disaggregated architecture).
    - Example 2: FPGA Shell for seamless host/accelerator <->accelerator communication.
- **SW**:
  - Suite of tools and SW developed for HPC and for enabling all digital laboratory's functionalities.
- **Coyote:** Performance Modeling tool for many-core accelerators.

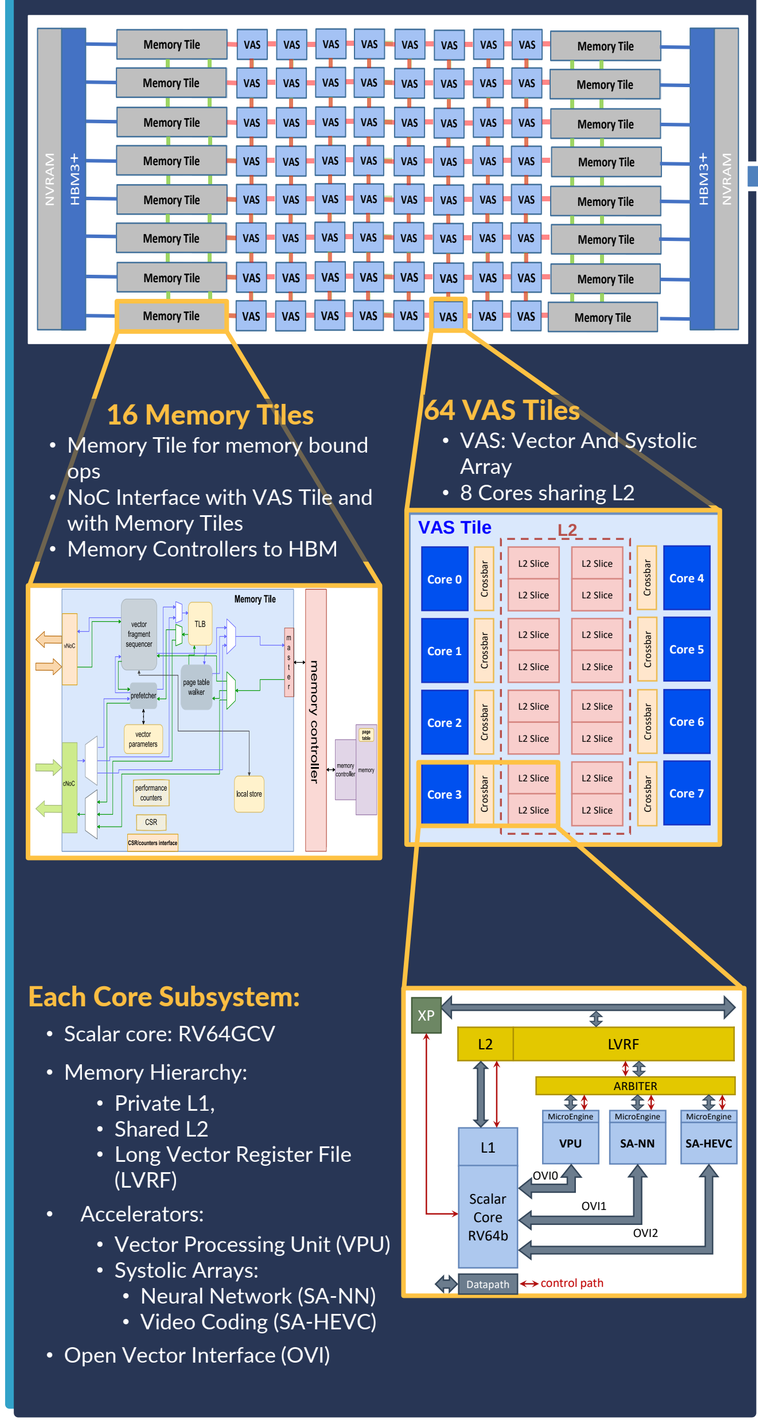
Connection of MEEP to a supercomputer facilities (@BSC).



WHAT IS ACME?

- **A**ccelerator **C**ompute and **M**emory **E**ngine
- Self-Hosted Accelerator for Exascale Systems
- Disaggregated Architecture:
  - Compute bound ops in VAS Tile
  - Memory bound ops in Mem Tile

ACME ARCHITECTURE

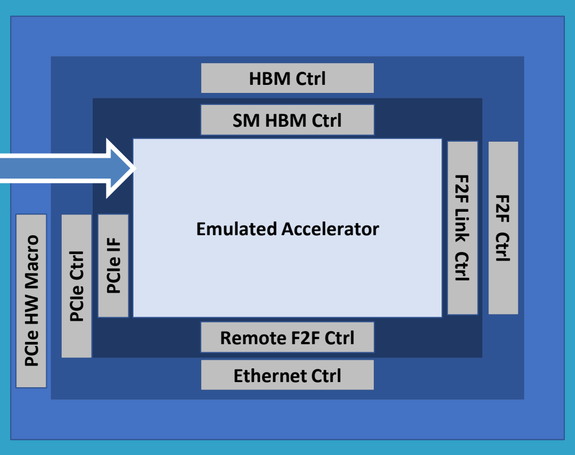


MEEP FPGA SHELL

- Flexible and extensible communication wrapper
- Architecture agnostic (already working with different Open-Source RISC-V based projects)

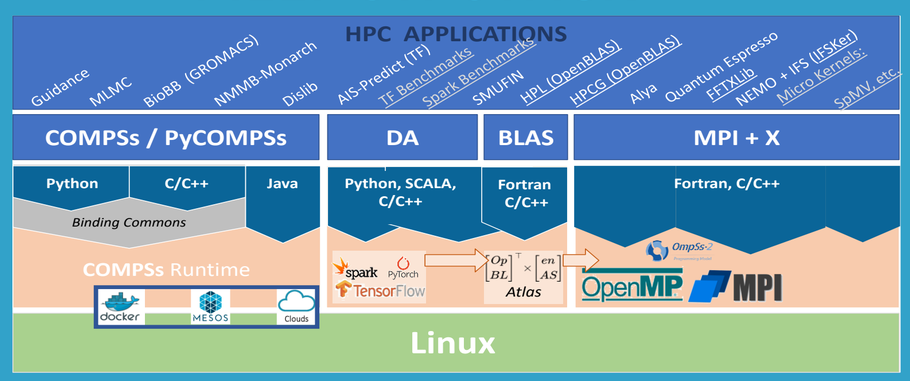
DRAC OpenPiton + Ariane RISC-V

- Standard communication interfaces between host/accelerator & accelerator.



- Supported IPs: PCIe (qdma/xdma), Aurora, Ethernet, HBM, DDR4, UART, ROM.
- Includes software drivers (host and accelerator sides) to ensure interaction between the hardware and the operating system.
- Project generation tool: automated FPGA flow process → implementation, deployment and acceptance tests for all the emulation accelerators, based on a Continuous Integration and Continuous Development (CICD).

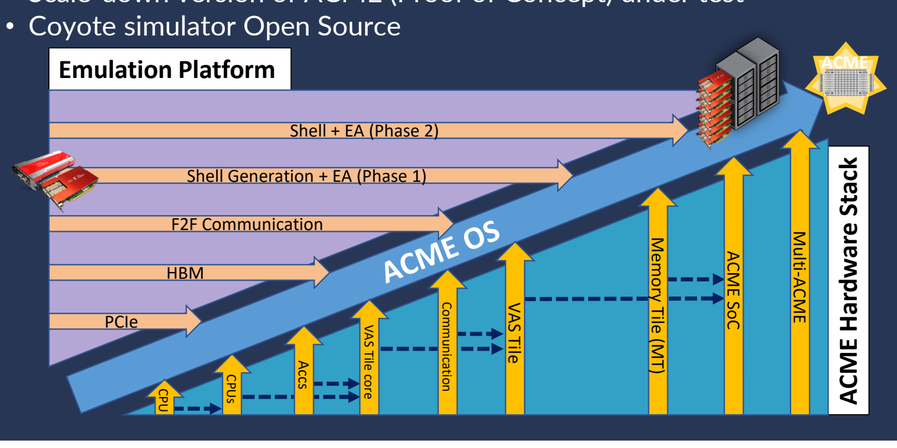
MEEP SW STACK



- Identified workloads to accelerate in MEEP platform
- SW Support at different levels
  - Compiler
  - Linux OS on ACME
  - Services & extensions for Host/FPGA communications

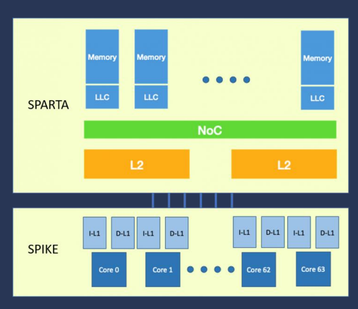
ROADMAP & STATUS

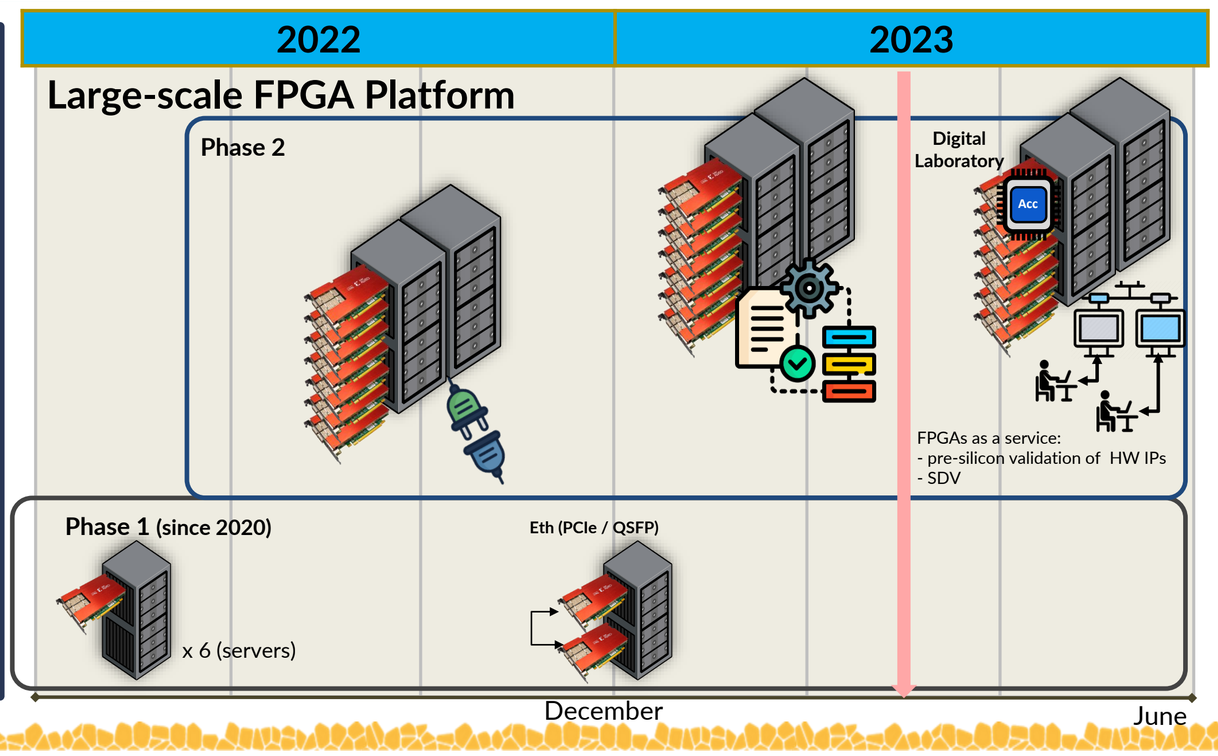
- Large-scale FPGA-based infrastructure available
- MEEP FPGA Shell Open Source
- SW releases Open Source
- Scale-down version of ACME (Proof of Concept) under test
- Coyote simulator Open Source



COYOTE

- Execution-driven simulator
- Based on Open Source RISC-V ISA
- Focused on data movement & modelling memory hierarchy
- Flexible, scalable and extensible
- Built upon Spike & Sparta





References:
[1] Fell, A., Mazure, D. J., Garcia, T. C., Perez, B., Teruel, X., Wilson, P., & Davis, J. D. (2021). *The MareNostrum Experimental Exascale Platform (MEEP).* Supercomputing Frontiers and Innovations, 8(1), 62–81. https://doi.org/10.14529/jsfi210105
[2] Perez, B., Fell, A., Davis, J. D.: *Coyote: An Open Source Simulation Tool to Enable RISC-V in HPC.* Design, Automation, and Test in Europe, DATE (2021)

EuroHPC Joint Undertaking

The MEEP Project has received funding from the European High-Performance Computing Joint Undertaking (JU) under grant agreement No 946002. The JU receives support from the European Union's Horizon 2020 research and innovation program and Spain, Croatia and Turkey

MEEP PARTNERS
Barcelona Supercomputing Center
Centro Nacional de Supercomputación
Faculty of Electrical Engineering and Computing
TÜBİTAK İLGEM

MEEP PROJECT FEEDBACK