



**Barcelona
Supercomputing
Center**
Centro Nacional de Supercomputación



**EXCELENCIA
SEVERO
OCHOA**

RISC-V, Enabling a Wide Open Future of HPC

John D. Davis, Ph.D.

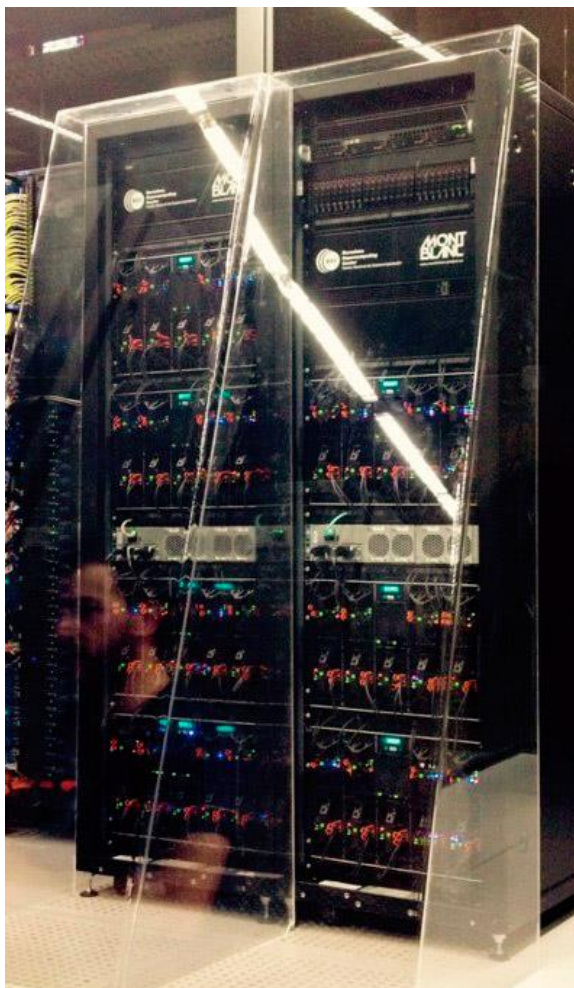
November 19, 2020

APPLEPIES 2020

An Open HPC Ecosystem?

- HPC Past
- HPC Present
- HPC Future
- LOCA

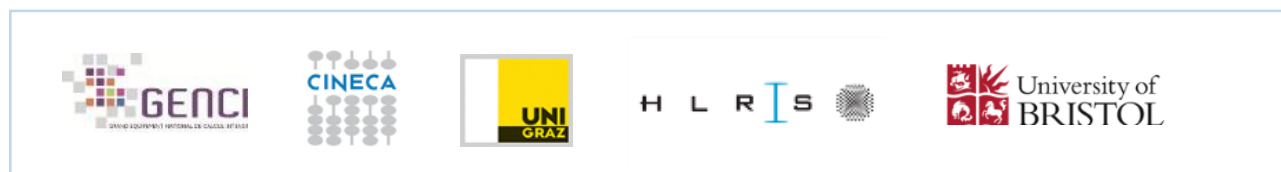
Mont-Blanc HPC Stack for ARM



Industrial applications



Applications



System software



Hardware



The Exascale Race – The Japanese example



Co-design from Apps to Architecture

- **Architectural Parameters to be determined**
 - #SIMD, SIMD length, #core, #NUMA node, O3 resources, specialized hardware
 - cache (size and bandwidth), memory technologies
 - Chip die-size, power consumption
 - Interconnect
- **We have selected a set of target applications**
- **Performance estimation tool**
 - Performance projection using Fujitsu FX100 execution profile to a set of arch. parameters.
- **Co-design Methodology (at early design phase)**
 1. Setting set of system parameters
 2. Tuning target applications under the system parameters
 3. Evaluating execution time using prediction tools
 4. Identifying hardware bottlenecks and changing the set of system parameters

Target applications representatives of almost all our applications in terms of computational methods and communication patterns in order to design architectural features.

Target Application	
Program	Brief description
① GENESIS	MD for proteins
② Genomon	Genome processing (Genome alignment)
③ GAMERA	Earthquake simulator (FEM in unstructured & structured grid)
④ NICAM+LETK	Weather prediction system using Big data (structured grid stencil & ensemble Kalman filter)
⑤ NTChem	molecular electronic (structure calculation)
⑥ FFB	Large Eddy Simulation (unstructured grid)
⑦ RSDFT	an ab-initio program (density functional theory)
⑧ Adventure	Computational Mechanics System for Large Scale Analysis and Design (unstructured grid)
⑨ CCS-QCD	Lattice QCD simulation (structured grid Monte Carlo)

The Exascale Race – The Japanese example

"Post-K" Arm64fx Processor is...

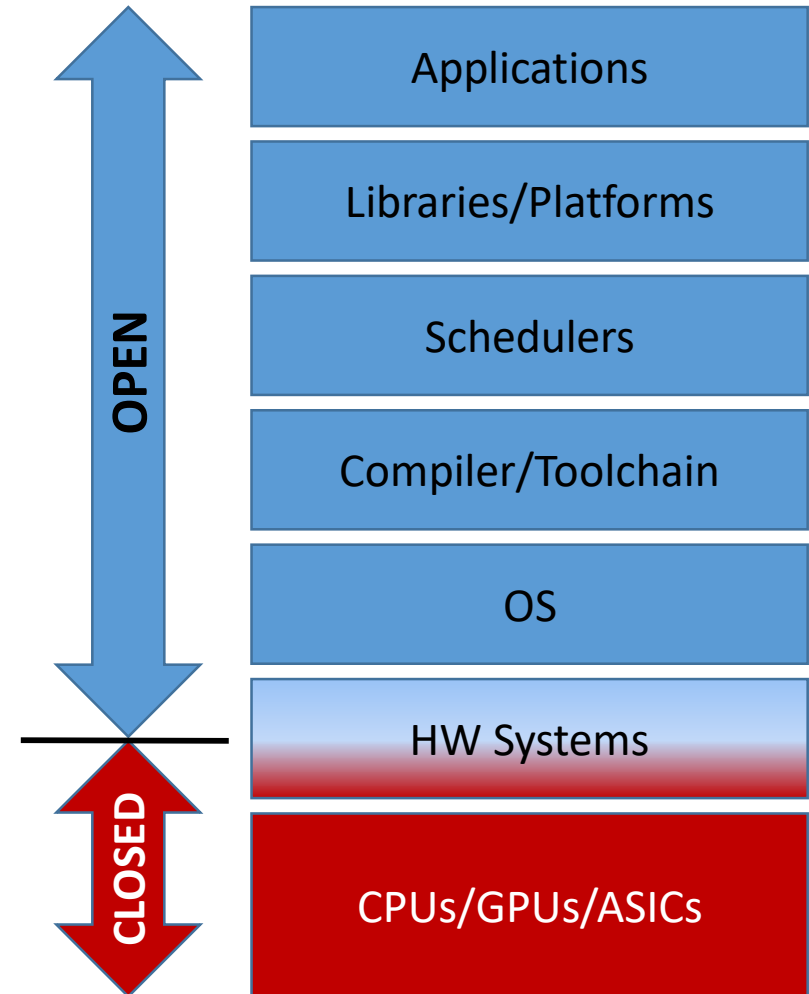
- an Many-Core ARM CPU...
 - 48 compute cores + 2 or 4 assistant (OS) cores
 - Brand new core design by Fujitsu
 - Near Xeon-Class Integer performance core
 - ARM V8.2 --- 64bit ARM ecosystem
- ...but also a GPU-like processor
 - SVE 512 bit vector extensions (ARM & Fujitsu)
 - Integer (1, 2, 4, 8 bytes) + float (16, 32, 64 bytes)
 - Cache + access localization (sector cache) – similar to scratchpad
 - IBM2 OPI – Massive Mem BW (1TByte/s, Bytes/DPF ~0.4 same as K)
 - Streaming memory access, strided access, scatter/gather etc.
 - Intra-chip barrier synch. and other memory enhancing features
 - 40GByte/s Tofu-.D interconnect + PCIe 3

#1 TOP500

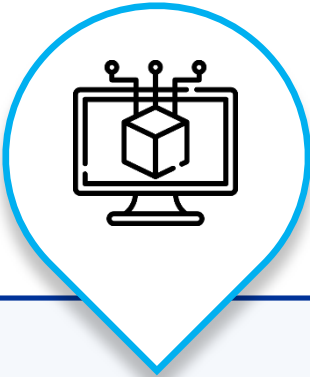
RIKEN logo in top left, RCCS logo in top right.

HPC Today

- Europe has led the way in defining a common open HPC software ecosystem
- **Linux** is the de facto standard OS despite proprietary alternatives
- Software landscape from Cloud to IoT already enjoys the benefit of open source
- Open source provides:
 - A common platform, specification and interface
 - Accelerates building new functionality by leveraging existing components
 - Lowers the entry barrier for others to contribute new components
 - Crowd-sources solutions for small and larger problems
- **What about Hardware and in particular, the CPU?**
- Inhibits opportunities in holistic co-design
 - Facing barrier to innovation
 - Being able to have a conversation or not



Today's technology trends



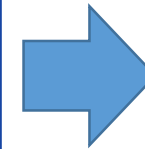
Massive penetration of Open Source Software

- IoT (Arduino),
- Mobile (Android),
- Enterprise (Linux),
- HPC (Linux, OpenMP, etc.)



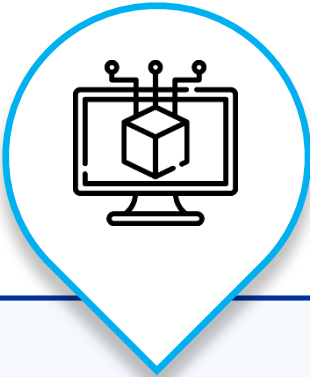
Moore's Law + Power =
Specialization

- More cost effective
- More performant
- Less Power



**SOFTWARE/
HARDWARE
CO-DESIGN**

Today's technology trends



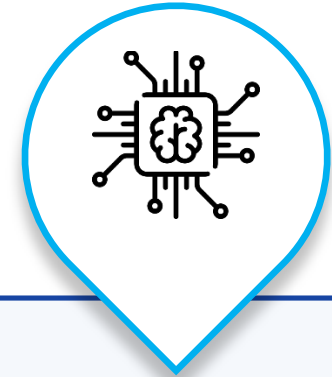
Massive penetration of Open Source Software

- IoT (Arduino),
- Mobile (Android),
- Enterprise (Linux),
- HPC (Linux, OpenMP, etc.)



Moore's Law + Power =
Specialization

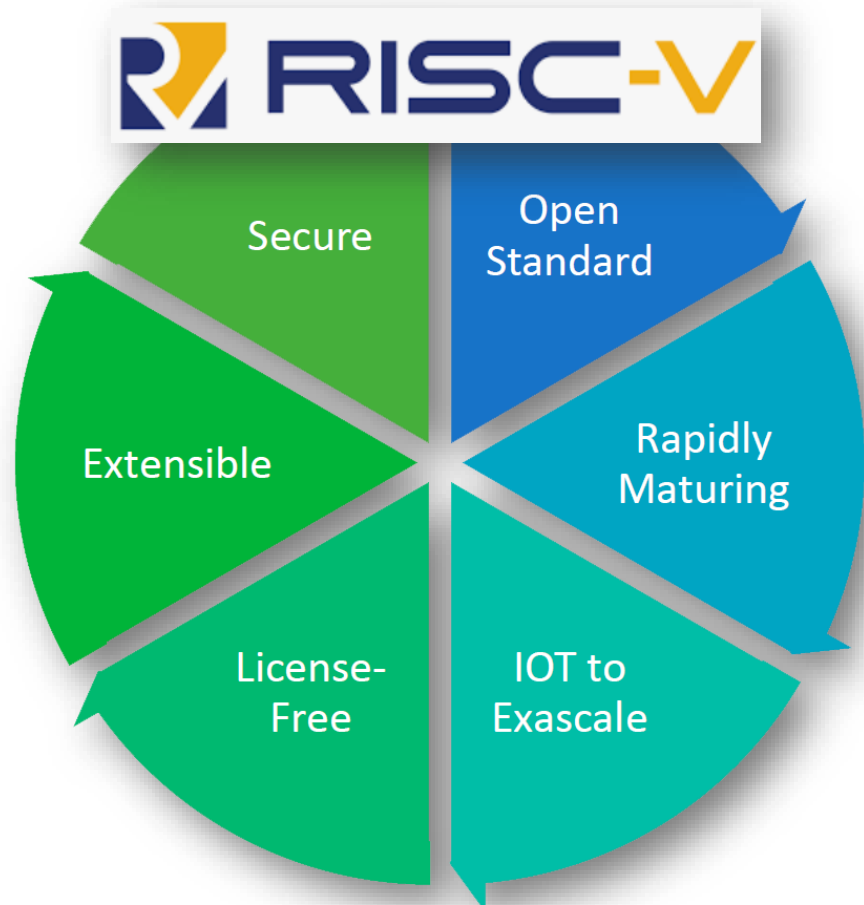
- More cost effective
- More performant
- Less Power



New Open Source Hardware
Momentum from IoT and the
Edge to HPC

- RISC-V
- OpenPOWER

RISC-V is democratizing chip-design

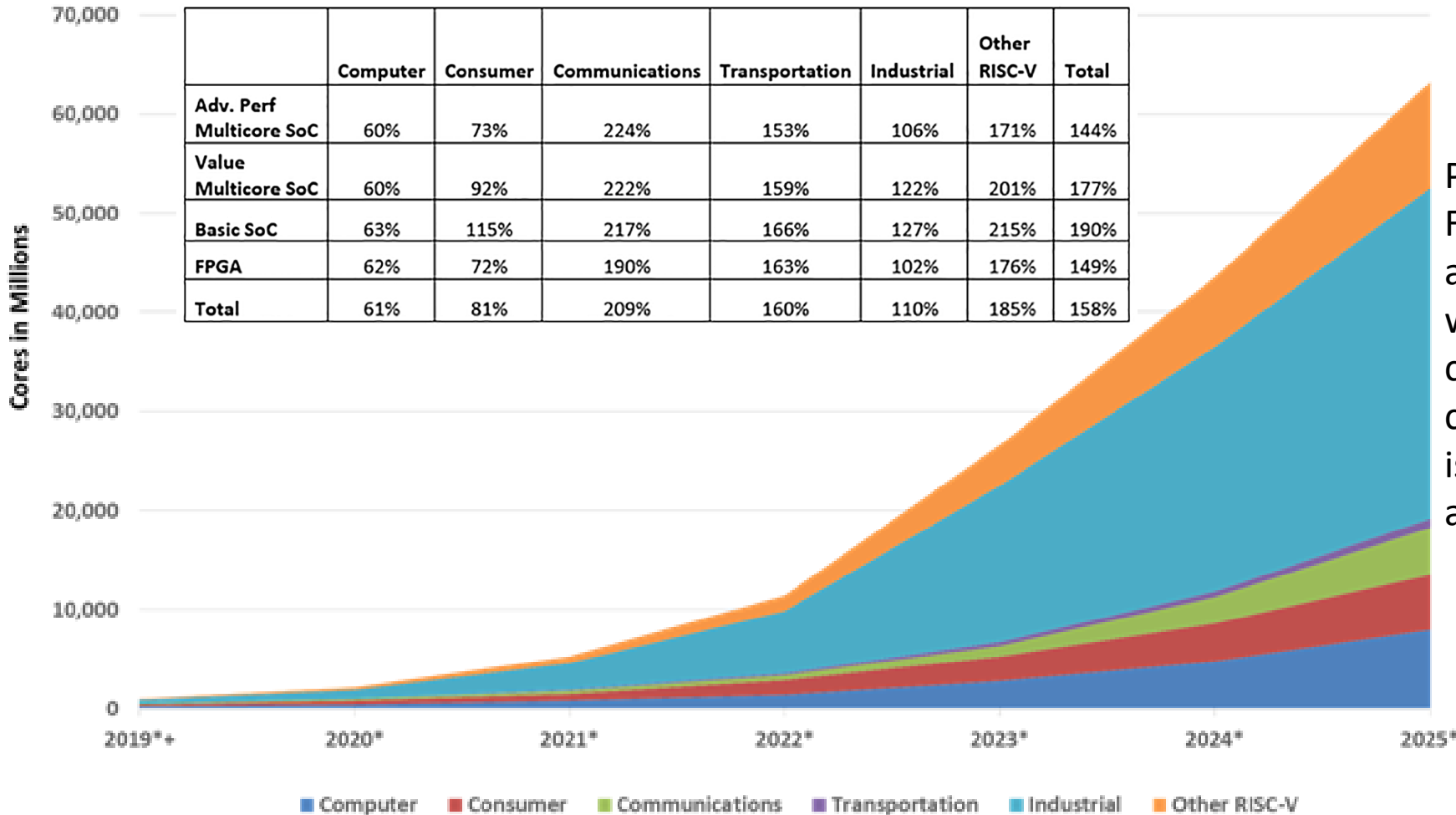


- ➔ More and more global IT actors are adopting RISC-V architectures to be vendor independent
 - ➔ Google
 - ➔ Amazon
 - ➔ Western Digital
 - ➔ Alibaba
- ➔ And of course the entire IoT ecosystem for lower performance, lower energy applications.
- ➔ Major opportunity for ICT industry also in Spain

RISC-V Worldwide Growth Projection

CAGR for RISC-V CPU cores between 2018 and 2025

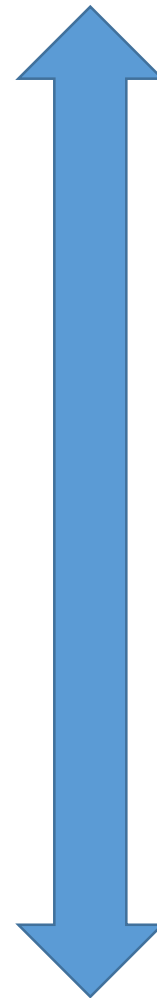
	Computer	Consumer	Communications	Transportation	Industrial	Other RISC-V	Total
Adv. Perf Multicore SoC	60%	73%	224%	153%	106%	171%	144%
Value Multicore SoC	60%	92%	222%	159%	122%	201%	177%
Basic SoC	63%	115%	217%	166%	127%	215%	190%
FPGA	62%	72%	190%	163%	102%	176%	149%
Total	61%	81%	209%	160%	110%	185%	158%



President of Semico Research, Jim Feldhan, commented: “Based on the already sizeable adoption of RISC-V, we forecast that the market will consume a total of 62.4 billion RISC-V cores by 2025, signaling that RISC-V is on the fast track to mainstream adoption.”

HPC Tomorrow

- Europe can lead the way to a completely **open SW/HW stack for the world**
- RISC-V provides the open source hardware alternative to dominating proprietary non-EU solutions
- Europe can achieve complete technology independence with these foundational building blocks
- Currently at the same early stage in HW as we were with SW when Linux was adopted many years ago
- **RISC-V can unify, focus, and build a new microelectronics industry in Europe.**



OPEN

GROMACS, NAMD,
WRF, VASP, etc.

OpenMP

COMPS

LLVM

Linux

OCP

RISC-V

Applications

Libraries/Platforms

Schedulers

Compiler/Toolchain

OS

HW Systems

CPUs/GPUs/ASICs

Open Source Beyond 2020



“Open Source has become mainstream across all software industry during the past 10 years. To a large extent, open software re-use has proven economically efficient. The level of maturity of Open Source Hardware (OSH) remains far lower than that of Open Source Software (OSS). However, business ecosystems for OSH are developing fast so that OSH could constitute a cornerstone of the future Internet of Things (IoT) and the future of computing.”

- DG Connect & DG IT Workshop, Brussels, Nov. 14-15, 2019

Source: <https://ec.europa.eu/digital-single-market/en/news/workshop-about-future-open-source-software-and-open-source-hardware>

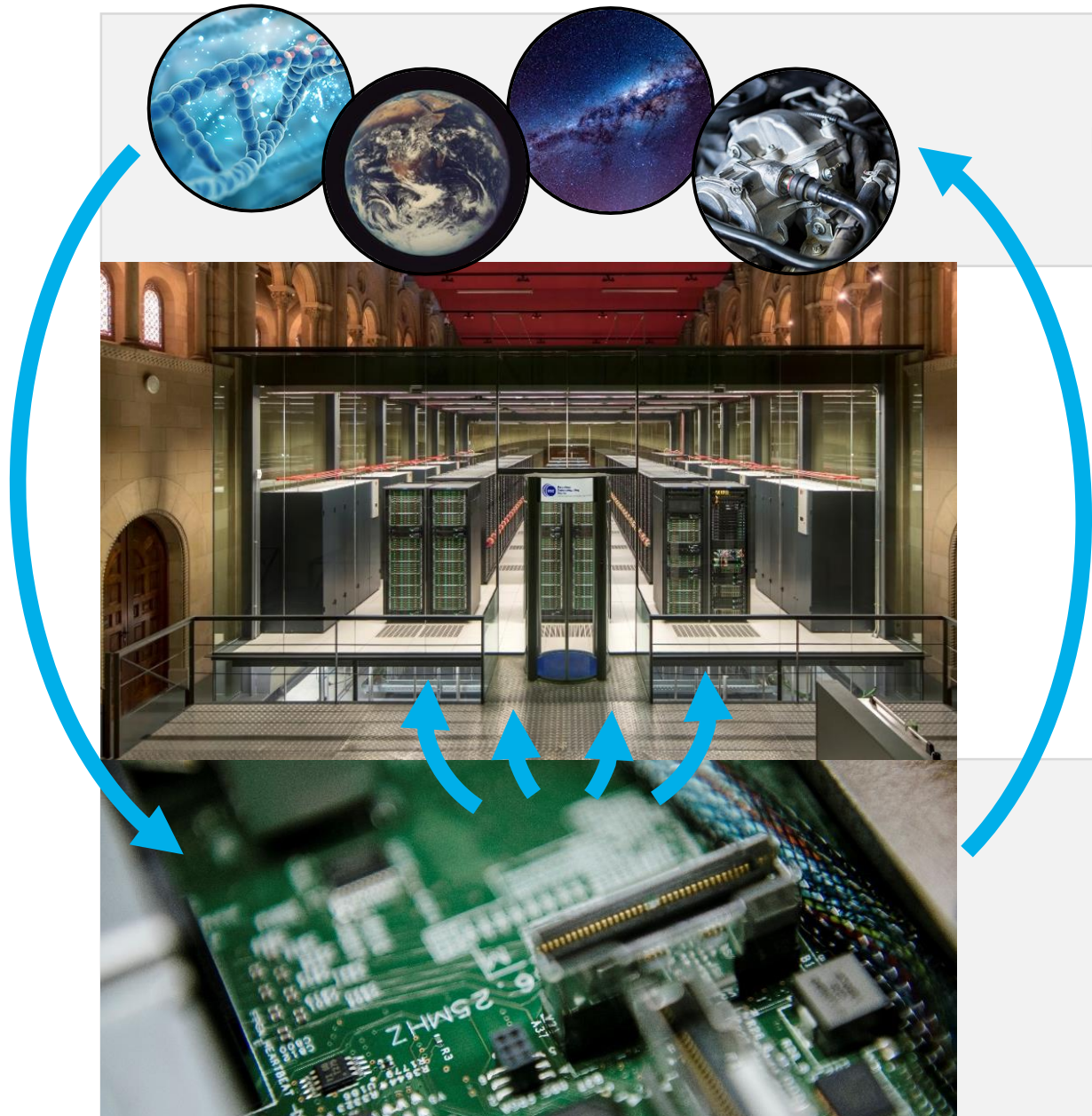
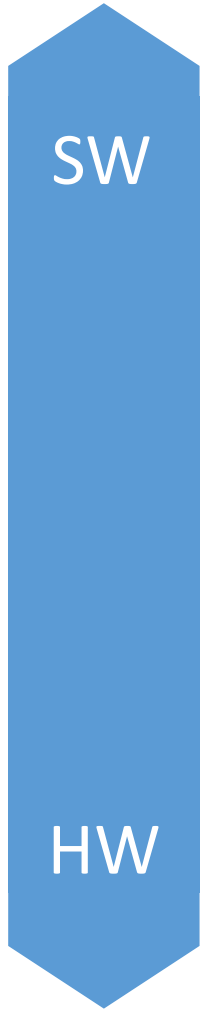
LOCA @ BSC



LOCA

European Laboratory for Open
Computer Architecture

BSC full stack



HPC Applications

Specialization using
HW/SW Co-Design

HPC Hardware



European Laboratory for Open
Computer Architecture



LOCA Goals

- Mechanism to extend open source ecosystem to include H/W
 - Add H/W expertise to BSC and European partners, leverage S/W expertise
 - Provide proven/usable Open Source H/W
 - Intersection of academia and industry
 - Open European IP repository → rapid implementation
 - Catalyst to reinvigorate European ICT industry
 - **Global** collaboration and training center
 - Incubator for European IP



European Collaboration & Education



Casteller

(human tower)



**Barcelona
Supercomputing
Center**
Centro Nacional de Supercomputación

Traditional chip design is done in a Master/Apprentice environment

LOCA recreates this environment by bringing in Masters from industry to collaborate with a variety of people, pushing beyond RTL

Professors, students, and industry veterans all together

Ideal sandbox for creative and innovative work

Research and Design to chip fabrication



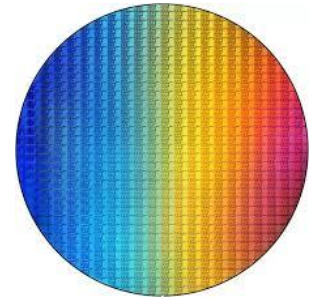
Rebuilding the European CPU Industry

Production

Closed + Open

Open

Research



Design

Exascale

eProcessor

EPI RISC-V
PILOT

MEEP

EPI

IP/Infra

IP/Infra

IP/Infra

IP/Infra



This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 826647



The MEEP project has received funding from the European High-Performance Computing Joint Undertaking (JU) under grant agreement No 946002. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Spain, Croatia, Turkey.



The Future is Wide Open!

- ➔ There is an urgent need, from mobile phones to supercomputers: more compute at lower power
- ➔ The RISC-V ecosystem is in the nascent period where it can become the de facto open hardware platform of the future
 - ➔ An opportunity for Europe to lead the charge to creating a full stack solution for everything, from supercomputers and HPC down to IoT devices
- ➔ Our main goal: Create European chips that meet the needs of future European and global markets across HPC, cloud, automotive, mobile to IoT
- ➔ **This is the framework for the Exascale Supercomputing Initiative at BSC**



A Successful EC Roadmap for the Future

- Embrace Open Source Hardware
 - Build infrastructure to support open source
 - Create an environment that links research to the ICT industry
 - Supported by DG Connect and other funding instruments
- Teach, train, and collaborate
- Leverage the Global Technology ecosystem
- Requires **SIGNIFICANT** funding for programs to build made in Europe IP
 - Many **focused** projects: Horizon Europe, Digital Europe, ...
 - Many **focused** teams: Collaborative IP and TRL development
 - Total and integrated vision for the future
 - Large Accelerator and CPU investment (> 1B€)



**Barcelona
Supercomputing
Center**
Centro Nacional de Supercomputación



Thank you

john.davis@bsc.es