



**Barcelona  
Supercomputing  
Center**  
Centro Nacional de Supercomputación



# Workshop on HPC & RISC-V and OpenPOWER

John D. Davis, BSC



**International Conference  
on Supercomputing 2020**

June 29 - July 2, 2020. Worldwide online event

Barcelona, 2020/06/29

# WELCOME to the ICS2020 Workshop: HPC & Open ISAs: OpenPOWER & RISC-V

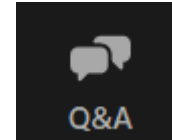
Start of the W&T		
8:30-9:00	John Davis (BSC) - <a href="#">bio</a>	Welcome and MEEP - <a href="#">abstract</a>
Session 1 / Chair: John Davis (BSC)		
9:00-9:30	Dan Petrisko (U. of Washington) - <a href="#">bio</a>	BlackParrot: An Agile Open Source RISC-V Accelerator Host Multicore - <a href="#">abstract</a>
9:30-10:00	Andrea Bartolini (U. of Bologna) - <a href="#">bio</a>	RISC-V open-ISA and open-HW - a Swiss army knife for HPC - <a href="#">abstract</a>
10:00-10:30	Anton Blanchard (Open Source Technology leader / Sidney, Australia OpenPOWER) - <a href="#">bio</a> and Tristan Gingold (CERN) - <a href="#">bio</a>	Microwatt and GHDL - An Open Hardware CPU written in VHDL, synthesized with Open Source tools - <a href="#">abstract</a>
Coffee break		
Session 2 / Chair: Alexander Fell (BSC)		
11:00-11:30	Borja Pérez (BSC) - <a href="#">bio</a>	Spike+Sparta: Developing a scalable RISC-V simulation infrastructure for HPC architectures. <a href="#">abstract</a>
11:30-12:00	Osman Unsal ( <a href="#">bio</a> ) and Adrián Cristal (BSC) - <a href="#">bio</a>	Designing open-source RISC-V hardware with open-source software - <a href="#">abstract</a>
12:00-12:30	Frank K. Gürkaynak (ETH Zurich) - <a href="#">bio</a>	Seven stories from seven years of PULP project - <a href="#">abstract</a>
12:30-13:00	Roger Espasa (SemiDynamics) - <a href="#">bio</a>	Hardening an academic core for industrial use - <a href="#">abstract</a>
Lunch break		

Session 3 / Chair: Borja Pérez (BSC)		
14:00-14:30	Brian Thompto (IBM Distinguished Engineer / IBM Systems / Austin OpenPOWER) - <a href="#">bio</a>	The Open Power ISA: A Summary of Architecture Compliancy Options and the Latest Foundations for Future Expansion - <a href="#">abstract</a>
14:30-15:00	Jose Moreira (IBM Research / NY OpenPOWER) - <a href="#">bio</a>	Advanced High-Performance Computing Features of the OpenPOWER ISA - <a href="#">abstract</a>
15:00-15:30	Francesc Moll ( <a href="#">bio</a> ) and Miquel Moretó (BSC) - <a href="#">bio</a>	Building the Road from Computer Architecture to Silicon at BSC - <a href="#">abstract</a>
Coffee break		
Session 4 / Chair: Miquel Moretó (UPC / BSC)		
16:00-16:30	James Kulina (Executive Director OpenPOWER) - <a href="#">bio</a>	OpenPower Foundation Update: New leadership and a bright open future - <a href="#">abstract</a>
16:30-17:00	Calista Redmond (CEO RISC-V International) - <a href="#">bio</a>	Growing RISC-V momentum around the world, in multiple disciplines, and across industries - <a href="#">abstract</a>
17:00-17:30	Krste Asanovic (UC Berkeley/SiFive) - <a href="#">bio</a>	RISC-V for HPC - <a href="#">abstract</a>
17:30-18:00	Jonathan Balkind (Princeton U.) - <a href="#">bio</a>	Enhancing the Open-Source P-Mesh Cache Coherence System for Open ISAs - <a href="#">abstract</a>
18:00-18:30	John Davis (BSC)	<b>Special Announcement &amp; Wrap-up</b>

# Today's Logistics

- Webinar will open 15 minutes before
- Sessions will be recorded and will be made available online
- We kindly ask you to mute your audio and do not use video

# Q&A



- Please, write your questions in the Q&A window. The session chairs will read them at the end of each talk for the speaker to answer.
- There will be coffee / lunch break out zoom links for each speaker after each session if they are available & you wish to continue the conversation.
- Links will be shared in the CHAT at the end of each session.



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# The Future is Wide Open!

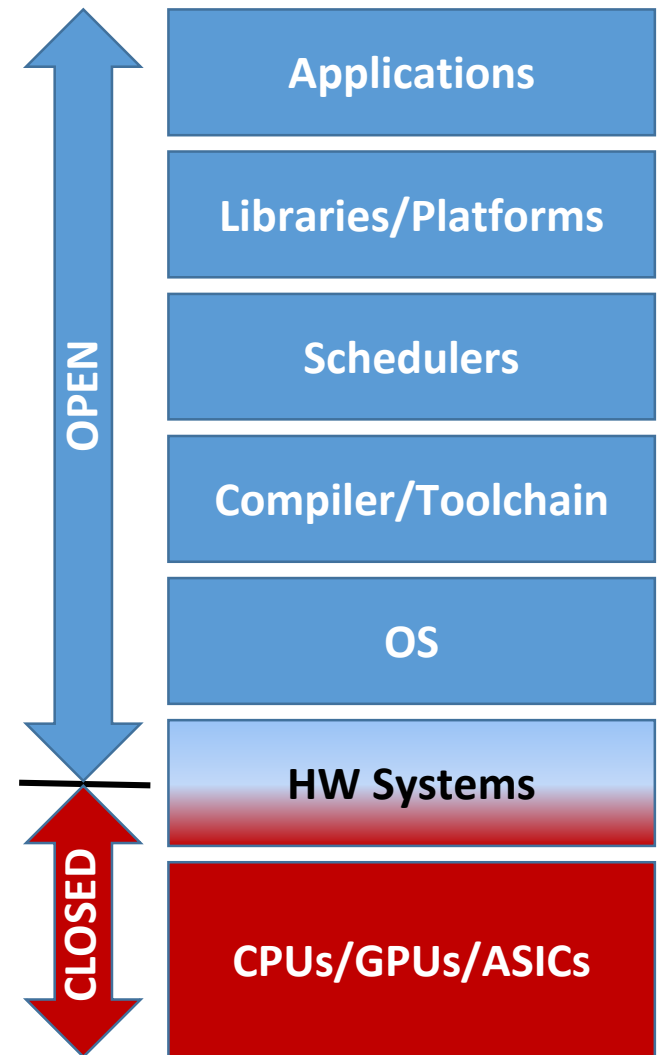
John D. Davis

2020/06/29

ICS 2020 Workshop: HPC & Open ISAs

# HPC today

- Europe has led the way in defining a common open HPC software ecosystem
- Linux is the de facto standard OS despite proprietary alternatives
- Software landscape from Cloud to IoT already enjoys the benefit of open source
- Open source provides:
  - A common platform, specification and interface
  - Accelerates building new functionality by leveraging existing components
  - Lowers the entry barrier for others to contribute new components
  - Crowd-sources solutions for small and larger problems
- **What about Hardware and in particular, the CPU and accelerators?**
  - Inhibits opportunities in holistic co-design
    - Facing barrier to innovation
    - Being able to have a conversation or not



# Today's Technology Trends



Massive penetration of Open Source Software

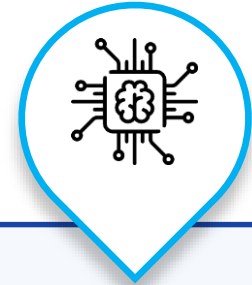
- IoT (Arduino),
- Mobile (Android),
- Enterprise (Linux),
- HPC (Linux, OpenMP, etc.)



Moore's Law + Power =

**Specialization**

- More cost effective
- More performant
- Less Power



New Open Source Hardware  
Momentum from IoT and the  
Edge to HPC  
RISC-  
• OpenPOWER  
**SOFTWARE/  
HARDWARE  
CO-DESIGN**

# Abbreviated Linux History

- 1991: Started development, release
- 1992: X Windows released
- 1998: Adopted by many major companies
- 2004: MareNostrum BSC Supercomputer OS
- 2009: Basis for many new business systems and the cloud
- 2013: Android in 75% of the world smart phones
- 2015: De facto OS for IoT, mobile, cloud, and supercomputers
- 2019: 86,1% of the smartphones, 67% of public servers, 75% of embedded systems ([\\*https://ec.europa.eu/digital-single-market/en/news/workshop-about-future-open-source-software-and-open-source-hardware](https://ec.europa.eu/digital-single-market/en/news/workshop-about-future-open-source-software-and-open-source-hardware))

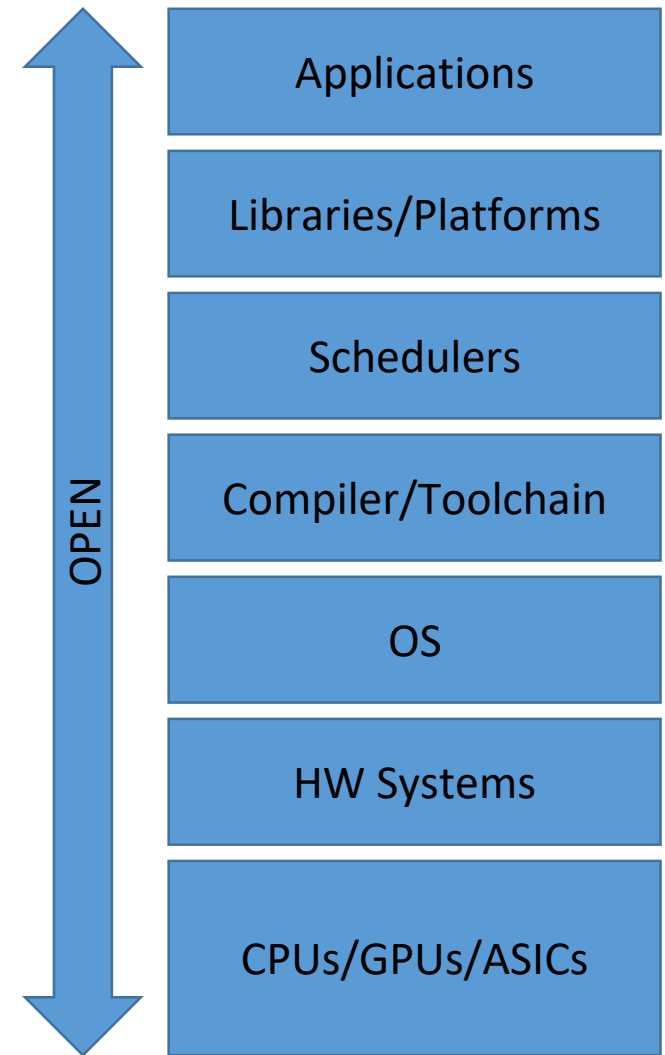
# RISC-V History

- 2010: Started development and initial proposal
- 2015: RISC-V Foundation formed
- 2019: Adopted by many major companies
  - Starting in the embedded market with already over 1 Billion CPUs
- 2020: RISC-V Foundation moves to Switzerland

The time is now to embrace and support RISC-V from IoT to HPC

# HPC tomorrow

- Open ISAs enable a completely open SW/HW stack/ecosystem for the world
- Open ISAs provide the open source hardware alternative to dominating proprietary non-EU solutions
- The world can achieve complete technology independence with these foundational building blocks
- Currently at the same early stage in HW as we were with SW when Linux was adopted many years ago
- Open Source ISAs and **ecosystems** can unify, focus, and build a new microelectronics industry.



# BSC Research using RISC-V

- Building **LOCA: European Laboratory for Open Computer Architecture**
  - Full stack co-design projects
  - Open Source Software + Hardware research
- Many projects, proposals and grants @ BSC to Support RISC-V
  - Horizon 2020: **EPI** SGA1
  - EuroHPC: **MEEP**, De-RISC, SELENE, eProcessor, ...
  - Others: **Lagarto**, **DRAC**, ESEL FRACTAL, ...
  - Need more calls need: multi-generation problem (SW + HW)
  - Collaboration with Microelectronics
  - Open Source Hardware Industrial Partners

# Open Source Beyond 2020



**“Open Source has become mainstream across all sectors of the software industry during the past 10 years. To a large extent, open software re-use has proven economically efficient. The level of maturity of Open Source Hardware (OSH) remains far lower than that of Open Source Software (OSS). However, business ecosystems for OSH are developing fast so that OSH could constitute a cornerstone of the future Internet of Things (IoT) and the future of computing.”**

*- DG Connect & DG IT Workshop, Brussels, Nov. 14-15, 2019*

[Source: https://ec.europa.eu/digital-single-market/en/news/workshop-about-future-open-source-software-and-open-source-hardware](https://ec.europa.eu/digital-single-market/en/news/workshop-about-future-open-source-software-and-open-source-hardware)

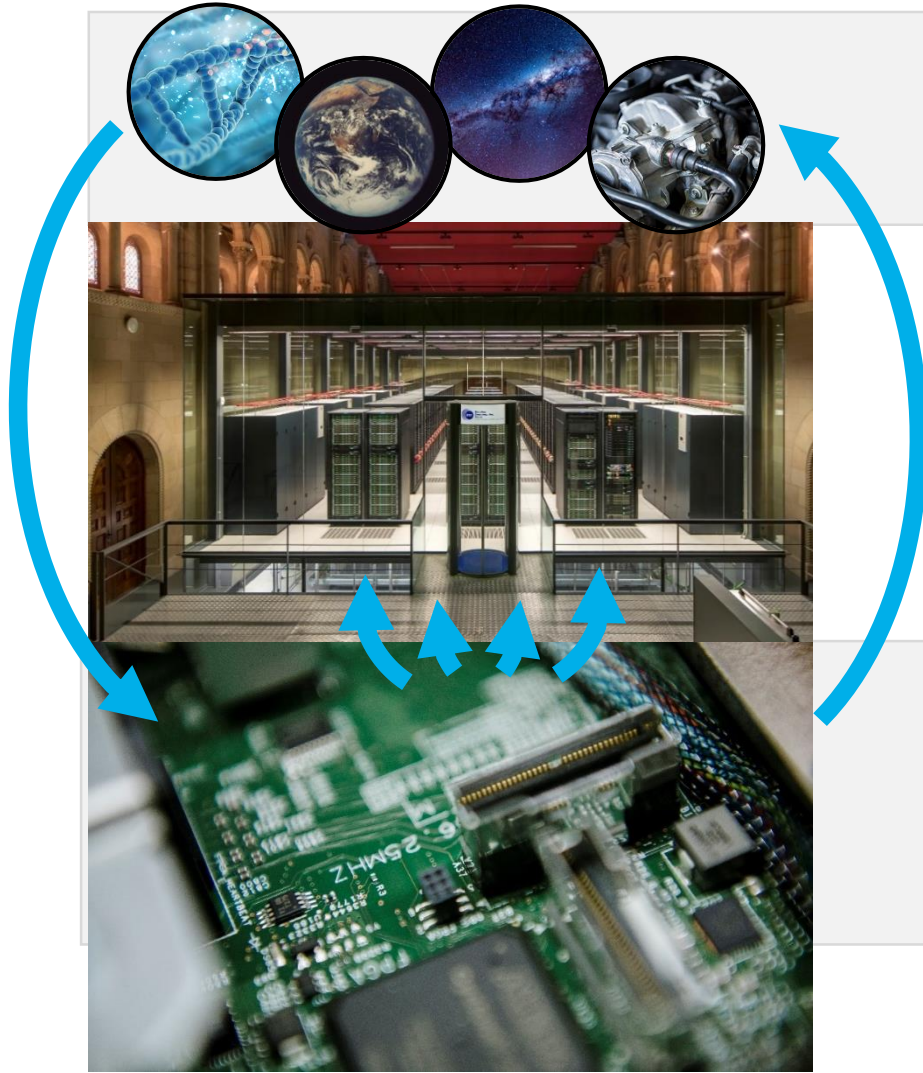
# LOCA @ BSC



LOCA

European Laboratory for Open  
Computer Architecture

# BSC full stack



HPC Applications

Specialization using  
HW/SW Co-Design



European Laboratory for Open  
Computer Architecture

HPC Hardware

# LOCA Goals

- Mechanism to extend open source ecosystem to include H/W
  - Add H/W expertise to BSC and European partners, leverage existing S/W expertise
  - Open European IP repository → rapid implementation
  - Provide proven/usable Open Source H/W
  - Intersection of academia and industry
  - Catalyst to reinvigorate European ICT industry Global collaboration and training center
  - Incubator for European IP



# European Collaboration & Education



**Casteller**  
(human tower)

Traditional chip design is done in a Master/Apprentice environment

LOCA recreates this environment by bringing in Masters from industry to collaborate with a variety of people, pushing beyond RTL

Professors, students, and industry veterans all together

Ideal sandbox for creative and innovative work

Research and Design to chip fabrication and software systems

# Come Build LOCA @ BSC



**Casteller**  
(human tower)



European Laboratory for Open  
Computer Architecture



European  
Open  
Hardware  
Architecture  
Initiative

We must stand on the shoulders of giants to build great things. We are assembling many giants and hope you can join us.



**MEEP**

MareNostrum Experimental  
Exascale Platform

# A Co-Design Laboratory: Building Infrastructure for Software and Hardware Research

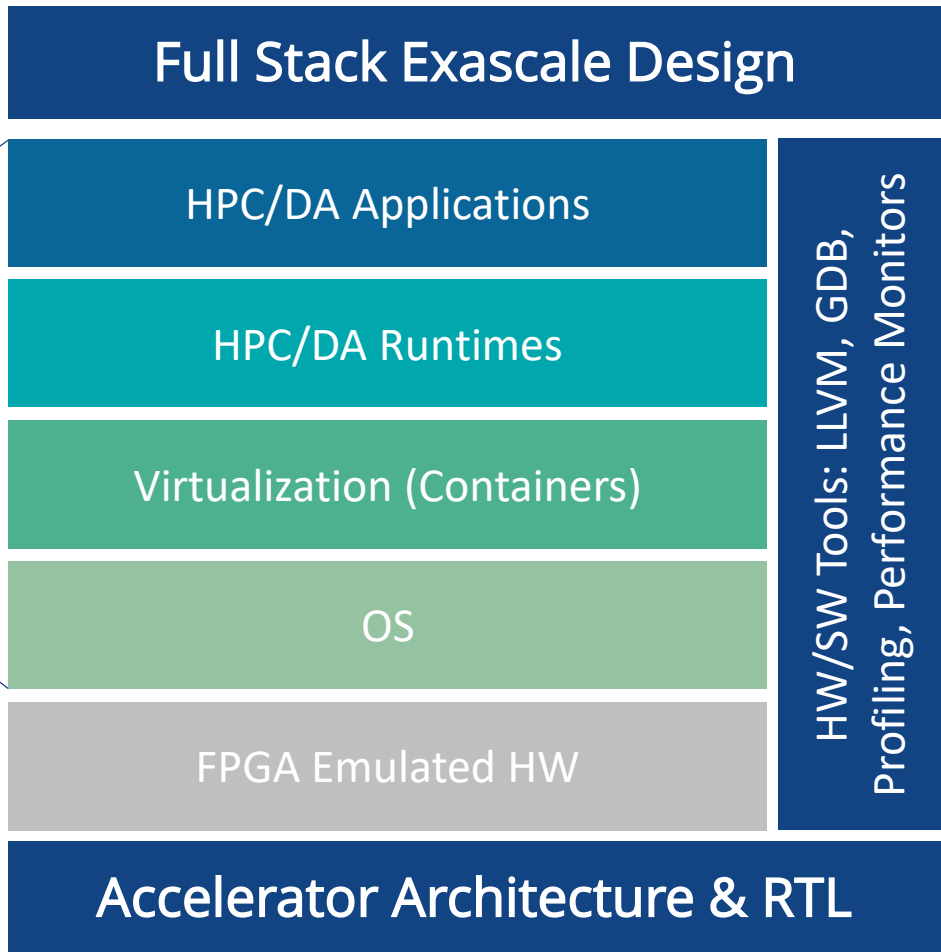
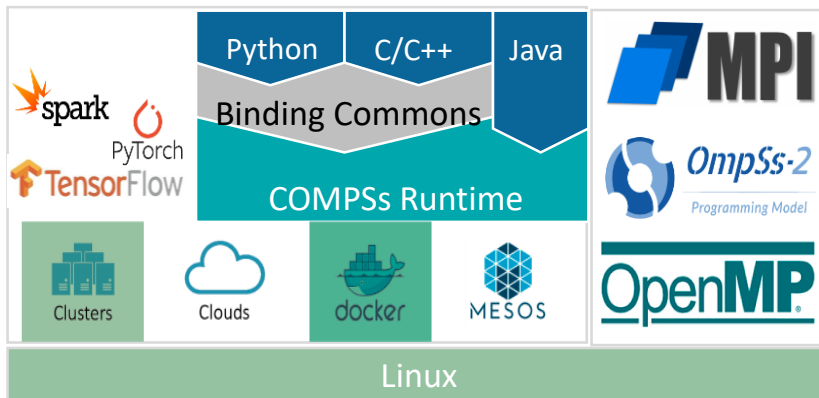
# MEEP Goals

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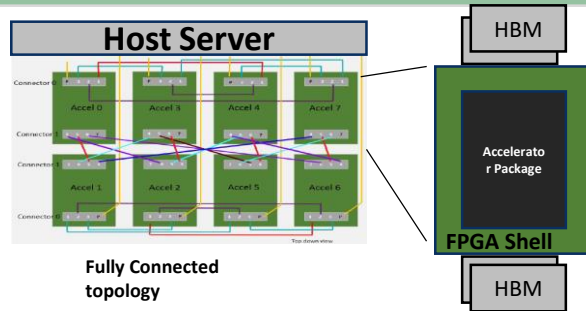
- What type of HPC Exascale accelerator would we build in 2025?
  - MEEP is a flexible FPGA-based emulation platform that will explore hardware/software co-designs for Exascale Supercomputers
    - Software Development Vehicle
    - An evaluation platform of pre-silicon IP and ideas, at speed and scale
      - Efficiently Map RTL to FPGAs (not gate2gate)
- Flexible and Reusable
  - Enable other SW and HW projects @ BSC and in the EU
    - Physical platform
    - Emulation IP
    - Open SW and HW IP

# MEEP in a Nutshell: A Co-Design Laboratory

1. Software Ecosystem
2. Hardware (RTL)
3. FPGAs



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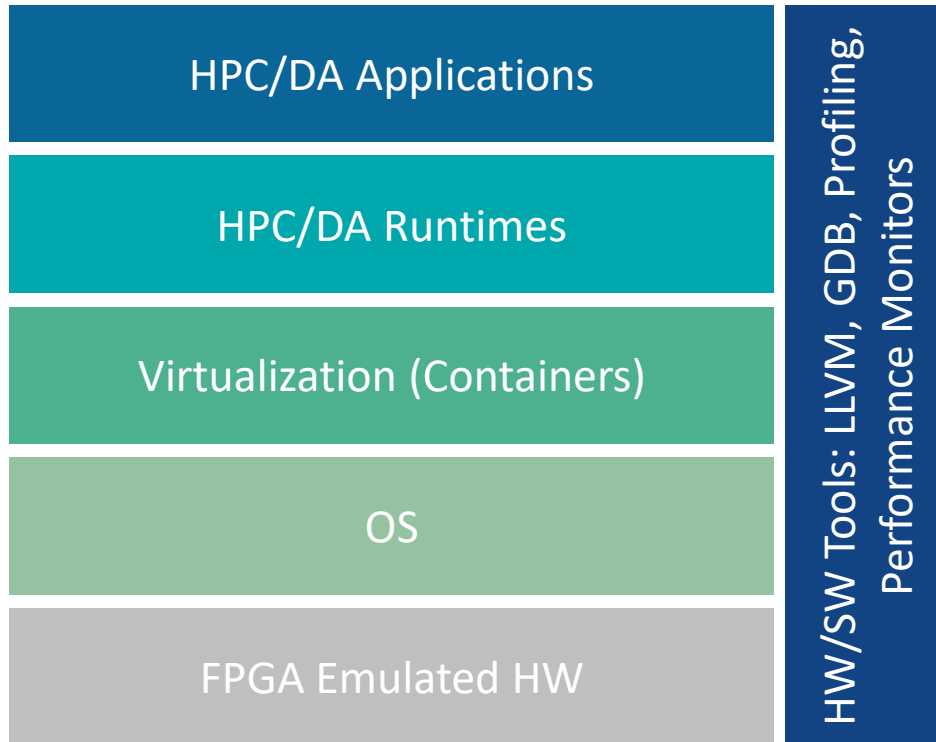


# MEEP Architecture & RTL

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- Good for Dense and **Sparse** compute
  - Dense sets # of FMAs
  - Sparse defines memory hierarchy
- Chiplet Architecture/Integration
  - 100- 150 mm<sup>2</sup> Chiplets
- Memory: Assuming HBM3+
- Architectures for Accelerator
  - Vector Lanes & VRF
  - Systolic Array
- Architecture Simulator (later today...)

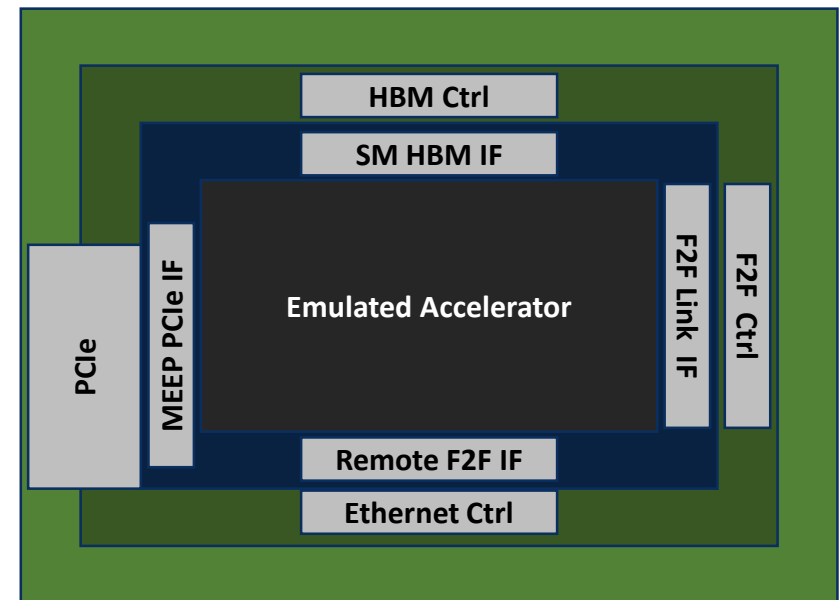
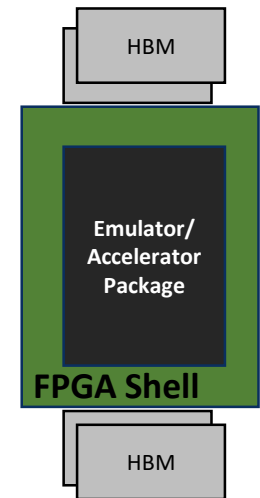
# MEEP RISC-V Software Ecosystem



- Traditional and emerging HPC/HPDA
  - Linpack, HPCG, GROMACS, AI/ML/DL
- OpenMP/MPI, COMPS, Apache Spark & TensorFlow
- Containers for Applications and Task
- Linux
- Programming Models
  - Offload vs Self-hosted
- Accelerator support in LLVM
- Profiling and tuning

# FPGA Shell RTL

- Standard External Interfaces
  - FPGA and Platform specific
  - Built on top of Vendor IP (PCIe, HBM, Ethernet, etc.)
- MEEP Shell Interfaces
  - Standardize Internal Interfaces (same across multiple FPGAs)
    - PCIe to the Host
    - FPGA-to-FPGA Interface
      - Local and remote addressing
    - HBM interface
      - Pseudo channel
      - Aggregate
    - Network interface (QSFP)



# FPGA SW

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- PCIe “Accelerator” Driver
  - Memory management (DMA)
  - Control
- Linux OS
  - Storage and network stacks
- RISC-V Software
  - Offload first
  - Self-hosted
- Tools, profiling, and debugging
  - SW and HW debugging support
  - Performance counters?
  - Partial reconfiguration?
    - Decouple FPGA shell from emulator

# MEEP Target Contributions

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## SW + HW → FPGA Emulator

1. MEEP will deliver a series of **Open-Source IPs**, when possible, that can be used for academic purposes and integrated into a functional accelerator or cores for traditional and emerging HPC applications.
2. MEEP will provide a foundation for building European-based chips and **infrastructure to enable rapid prototyping** using a library of IPs and a standard set of interfaces to the Host CPU and other FPGAs in the system using the FPGA shell.
3. MEEP will use the RISC-V Open ISA and **improve the RISC-V hardware and software ecosystem** using a software/hardware co-design approach starting with suite of traditional and emerging HPC applications, software tool chain down to specialized hardware.



# MEEP

MareNostrum Experimental  
Exascale Platform

[www.meep-project.eu](http://www.meep-project.eu)

[john.davis@bsc.es](mailto:john.davis@bsc.es)

**Session 1 / Chair: John Davis (BSC)**

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**BlackParrot:**

**An Agile Open Source RISC-V  
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Microwatt and GHDL - An Open Hardware  
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Open Source tools

# Coffee break 10:30-11:00

Please, join the links for the coffee breaks from  
10:30 to 11:00

One link per speaker

# Session 1 Chats...

- **John Davis:**

<https://us02web.zoom.us/j/81820066905?pwd=WXIKbEUzMTJXSndHM3h4eDBIT0l6Zz09>

Meeting ID: 818 2006 6905

Password: 356594

- **Anton Blanchard & Tristan Gingold :**

<https://us04web.zoom.us/j/74767023141?pwd=QUg5OUhncEZhMDZRYUpmZG1EOVhmdz09>

Meeting ID: 747 6702 3141

Password: 2QP6DM

- **Andrea Bartolini:**

<https://zoom.us/j/94199434046?pwd=K1hRcFNqVkh0N25JQXVnQUd4SHpSUT09>

Meeting ID: 941 9943 4046

Password: 861128

- **Dan Petrisko:**

<https://zoom.us/j/99740110441?pwd=SkxCTGprK3hNOTN6M1pPN2lnamZnUT09>

Meeting ID: 997 4011 0441

Password: 375118



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# Thank you

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