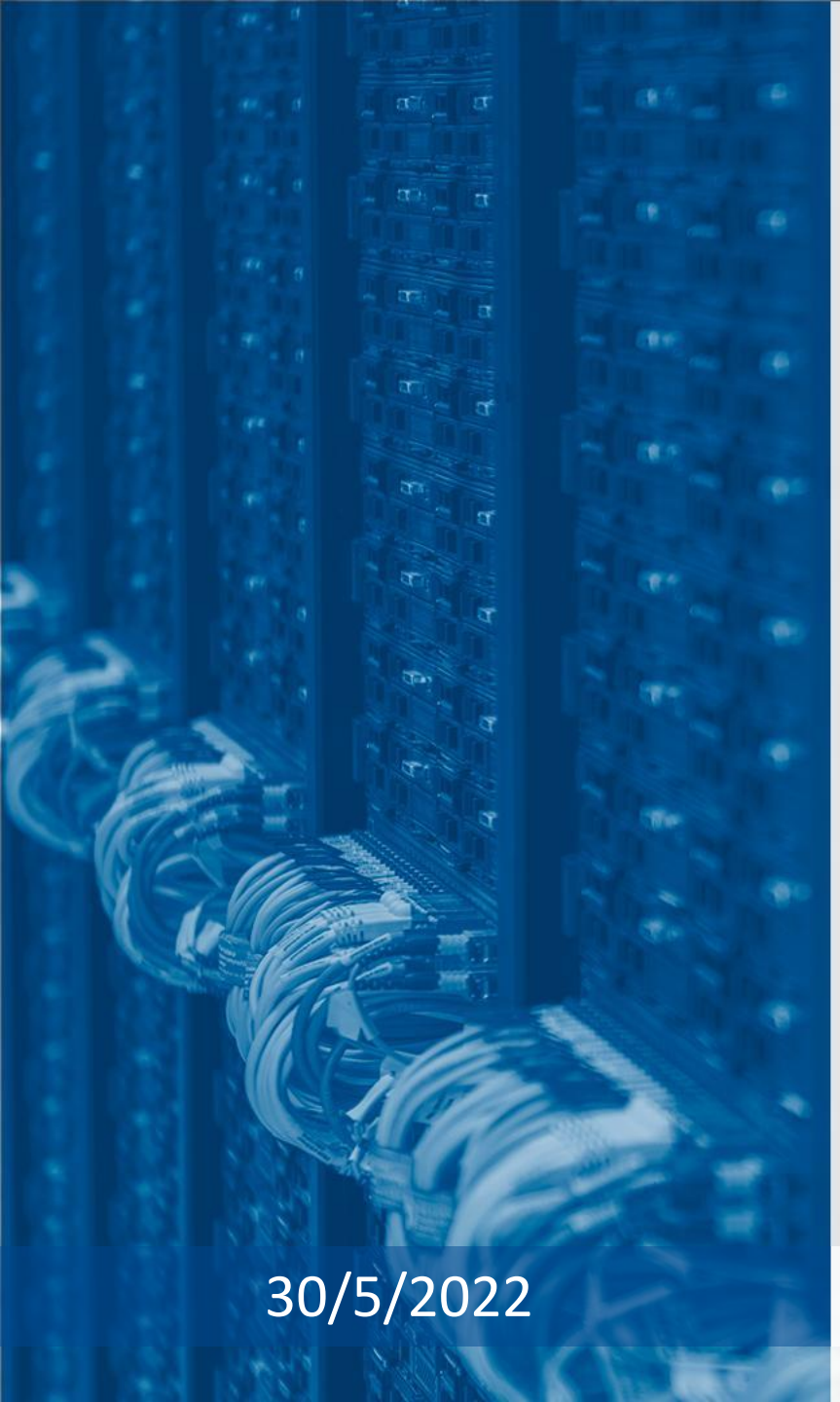


Barcelona Supercomputing Center
Centro Nacional de Supercomputación

MEEP
MareNostrum Experimental Exascale Platform

Creating an Open HPC Ecosystem with RISC-V

30/5/2022

BoF @ ISC'22

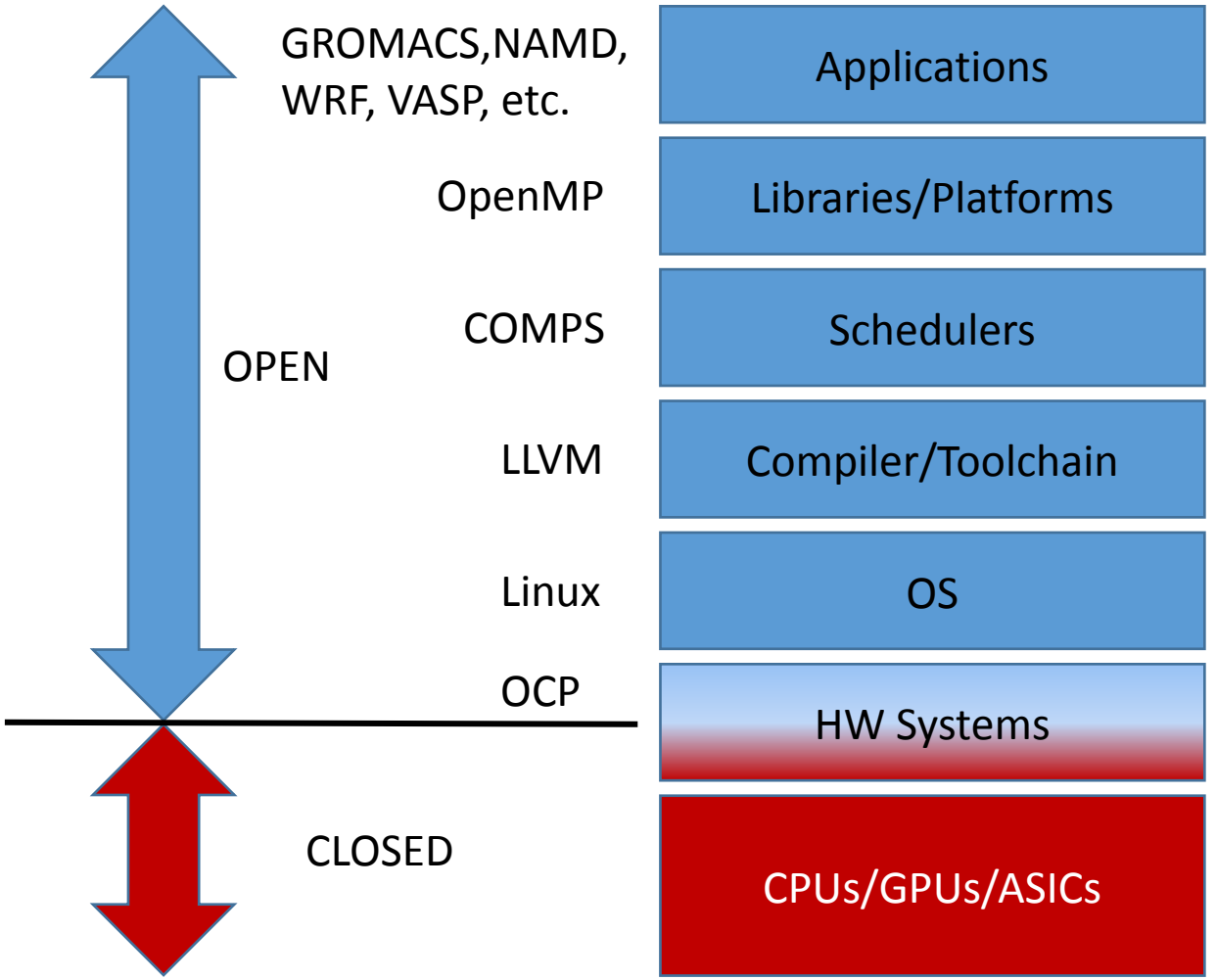
Overview

- Technology Trends
- What is RISC-V?
- SIG-HPC
- Getting Started
- Next talks...
- Discussion

Technology Trends

HPC Today

- **Europe has led the way in defining a common open HPC software ecosystem**
- **Linux** is the de facto standard OS despite proprietary alternatives
- Software landscape from Cloud to IoT already enjoys the benefit of open source
- Open source provides:
  - A common platform, specification and interface
  - Accelerates building new functionality by leveraging existing components
  - Lowers the entry barrier for others to contribute new components
  - Crowd-sources solutions for small and larger problems
- **What about Hardware and in particular, the CPU?**



RISC-V®

Today´s technology trends

Massive penetration of Open Source Software

- IoT (Arduino),
- Mobile (Android),
- Enterprise (Linux),
- HPC (Linux, OpenMP, etc.)

Moore´s Law + Power =

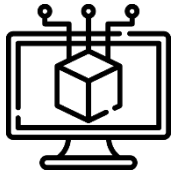
Specialization

- More cost effective
- More performant
- Less Power

SOFTWARE/
HARDWARE
CO-DESIGN

RISC-V®

Today´s technology trends



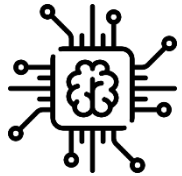
Massive penetration of Open Source Software

- IoT (Arduino),
- Mobile (Android),
- Enterprise (Linux),
- HPC (Linux, OpenMP, etc.)

Moore´s Law + Power =

Specialization

- More cost effective
- More performant
- Less Power



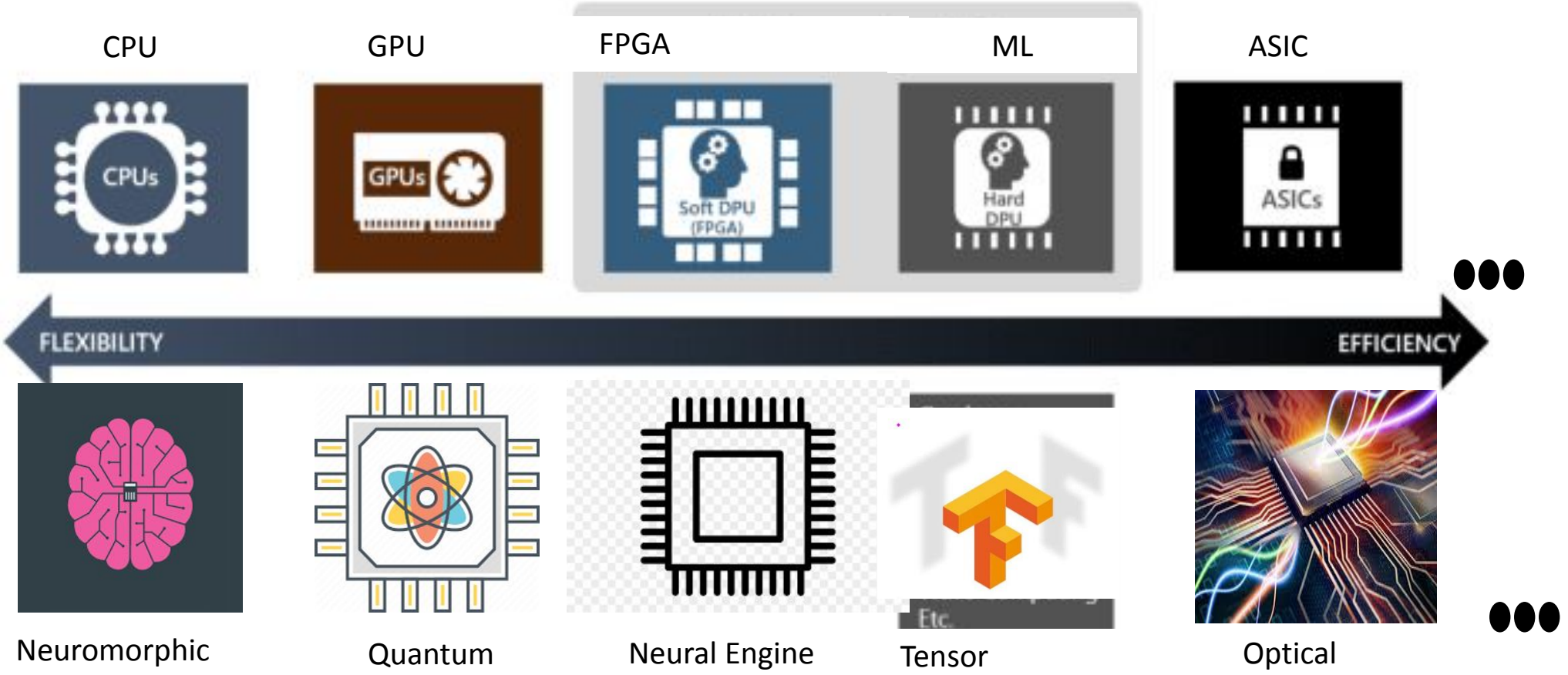
New Open Source Hardware Momentum from IoT and the Edge to HPC

- RISC-V
- OpenPOWER

RISC-V®

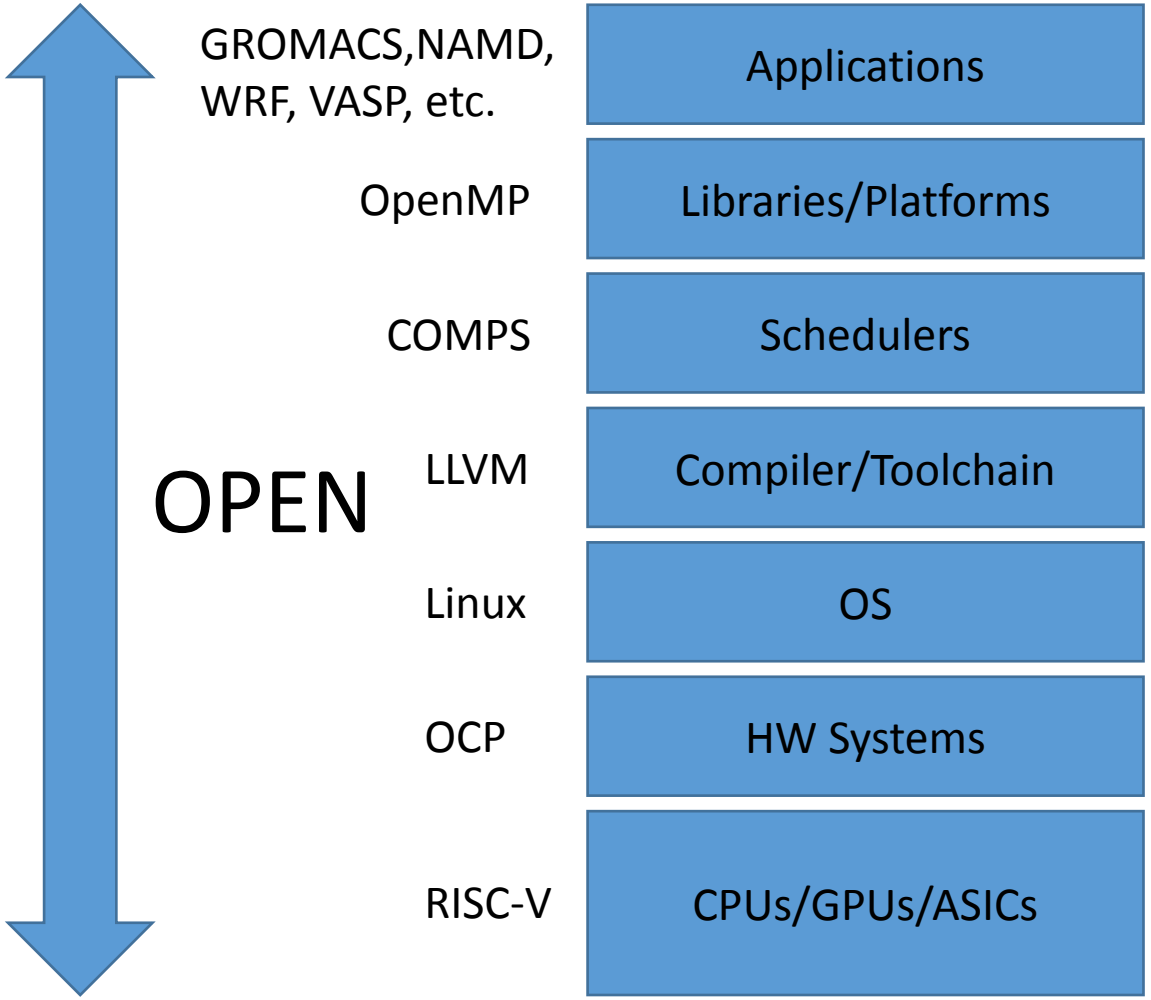
Future HPC Systems Will be Customized…

- You will be able to dial up what you need in your computer for your application mix …



HPC Tomorrow

- Europe can lead the way to a completely **open SW/HW stack for the world**
- RISC-V provides the open source hardware alternative to dominating proprietary non-EU solutions
- Europe can achieve complete technology independence with these foundational building blocks
- Currently at the same early stage in HW as we were with SW when Linux was adopted many years ago
- **RISC-V can unify, focus, and build a new microelectronics industry in Europe.**



RISC-V®

Why Open Source Hardware?

Software: Leverage a large ecosystem compatible across implementations
Security: A fully auditable collection of IPs: processors, accelerators, etc.
Safety: No black-boxes
SWaP & Customization: SW/HW co-design for exact feature match
Performance: State-of-the-art implementations
No vendor lock-in: Ecosystem to enable custom develop from SME to large enterprise
Sovereignty: Freedom of access and implementation from design to production
Open Collaboration: Faster time to market, community, leverage existing open source

What is RISC-V?

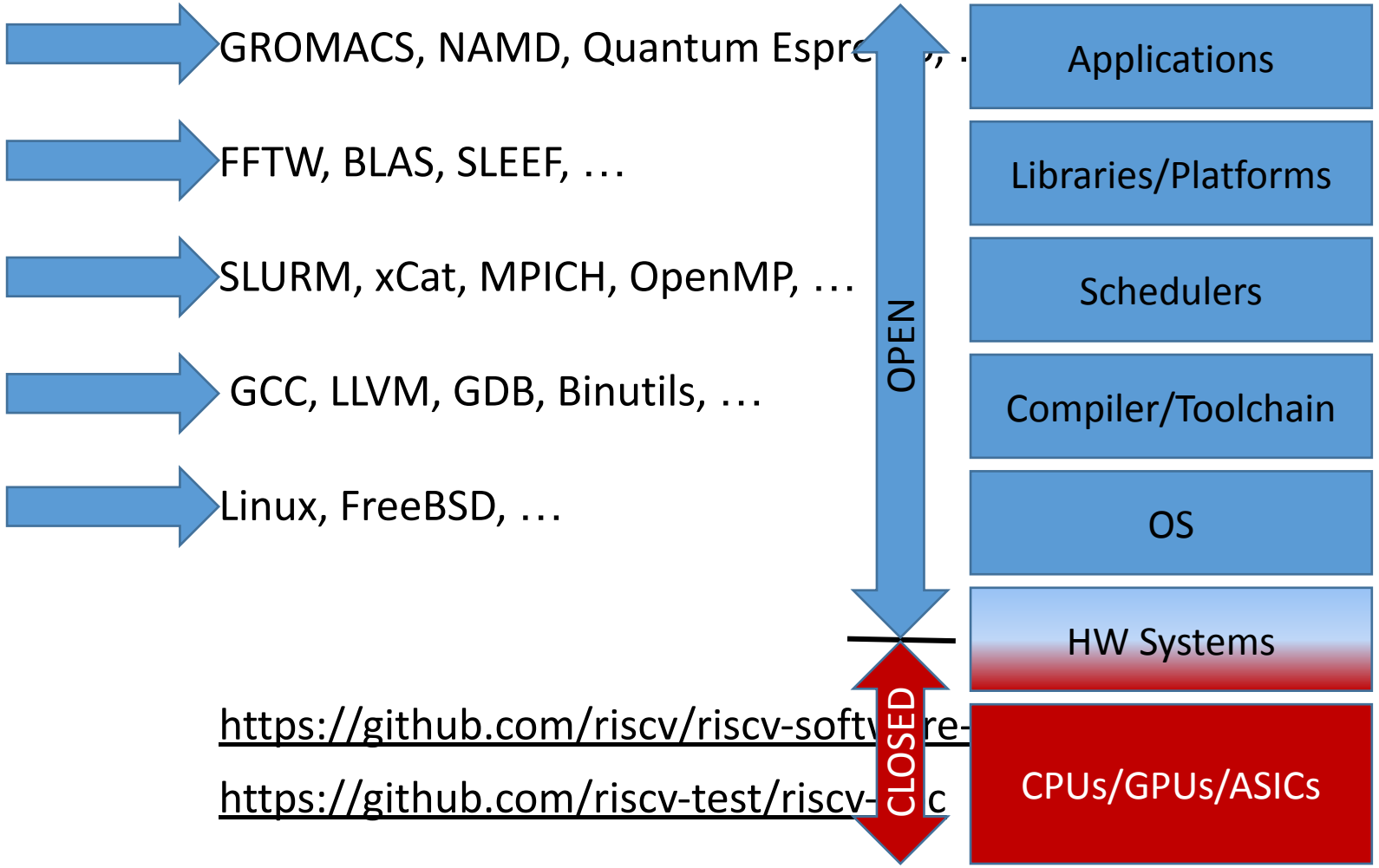
What is an ISA?

- An **Instruction Set Architecture (ISA) is part of the abstract model of a computer** that defines how the CPU is controlled by the software. The ISA acts as an interface between the hardware and the software, specifying both what the processor is capable of doing as well as how it gets done.
- The **ISA** provides the only way through which a user is able to interact with the hardware. It can be viewed as a **programmer's manual** because it's the portion of the machine that is visible to the assembly language programmer, the compiler writer, and the application programmer.
- The **ISA defines the supported data types, the registers, how the hardware manages main memory, key features (such as virtual memory), which instructions a microprocessor can execute, and the input/output model** of multiple ISA implementations. The ISA can be extended by adding instructions or other capabilities, or by adding support for larger addresses and data values.
- CPUs/devices that execute the instructions are an implementation of the ISA
    - ARM, MIPS, SPARC, Power, OpenPOWER, **RISC-V**, x86, etc...

RISC-V History

- 2010: Started development and initial proposal @ UC Berkeley
- 2015: RISC-V Foundation formed
- 2019: Adopted by many major companies
  - Starting in the embedded market with already over 1 Billion CPUs
  - RISC-V Foundation moves to Switzerland
- 2021:
  - **12,000,000,000+** Cores shipped

Open Ecosystem HW/SW Co-Design



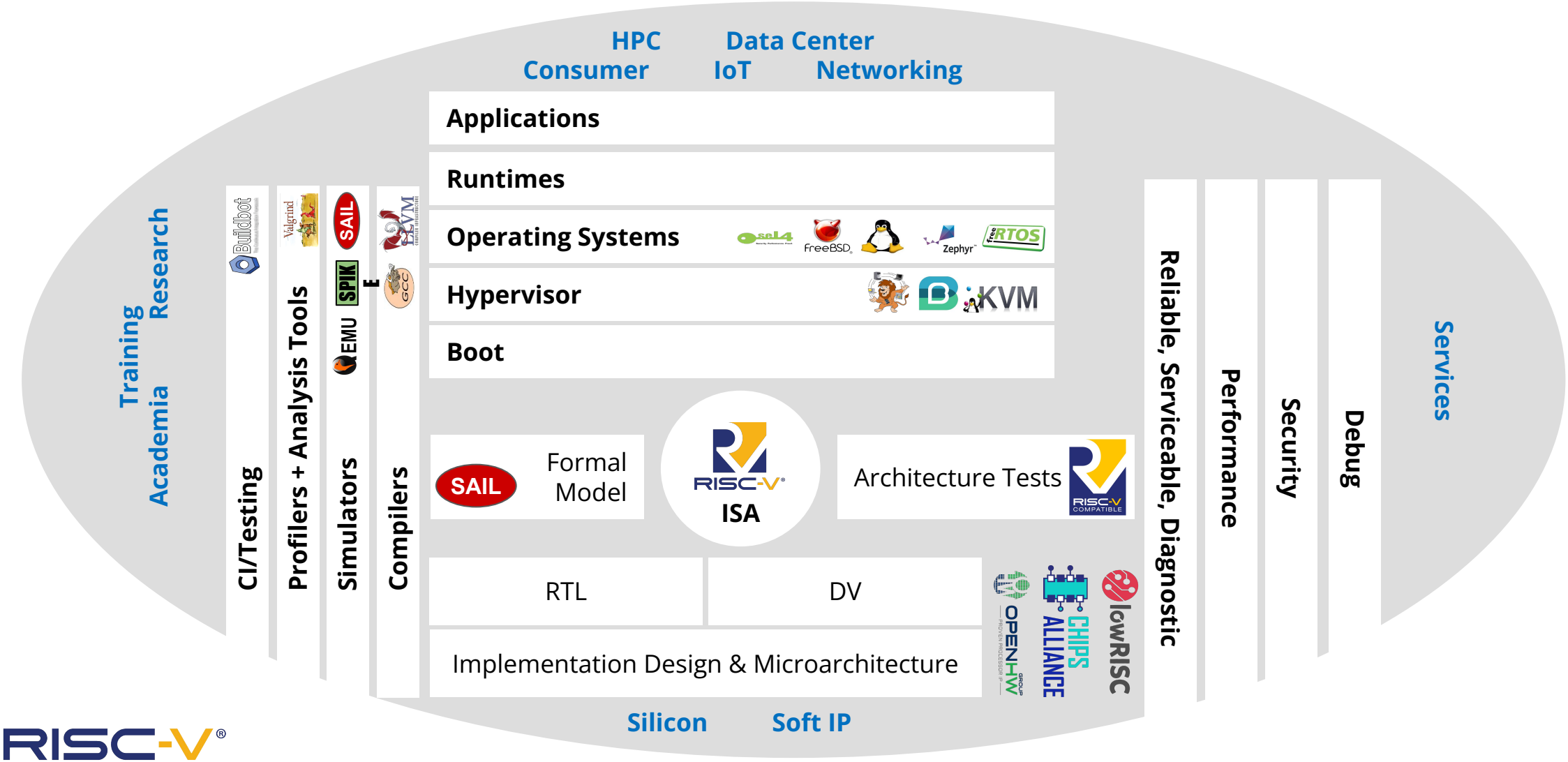
https://github.com/riscv/riscv-softw re-

https://github.com/riscv-test/riscv- c

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

RISC-V®

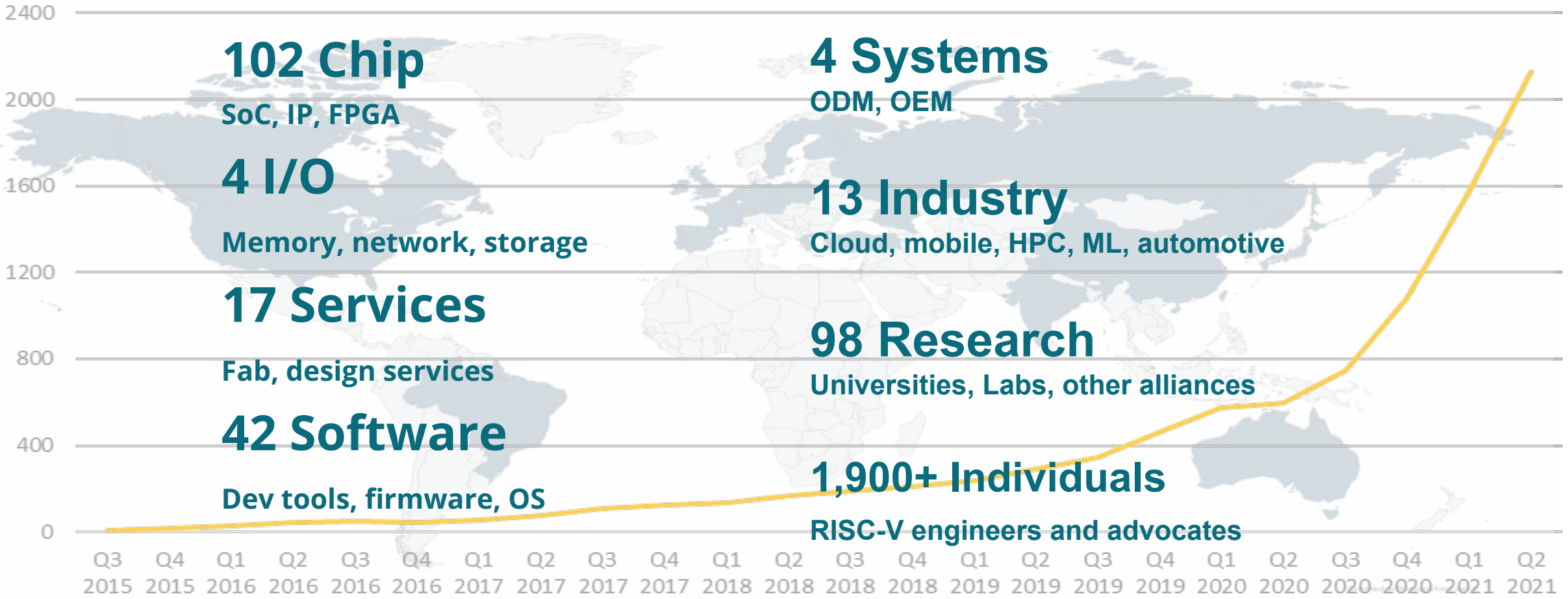
RISC-V Ecosystem



RISC-V®

More than 2,200 RISC-V Members

across 70 Countries



102 Chip
SoC, IP, FPGA

4 I/O
Memory, network, storage

17 Services
Fab, design services

42 Software
Dev tools, firmware, OS

4 Systems
ODM, OEM

13 Industry
Cloud, mobile, HPC, ML, automotive

98 Research
Universities, Labs, other alliances

1,900+ Individuals
RISC-V engineers and advocates

RISC-V membership grew 133% in 2020.
In 2021, RISC-V membership has already doubled.

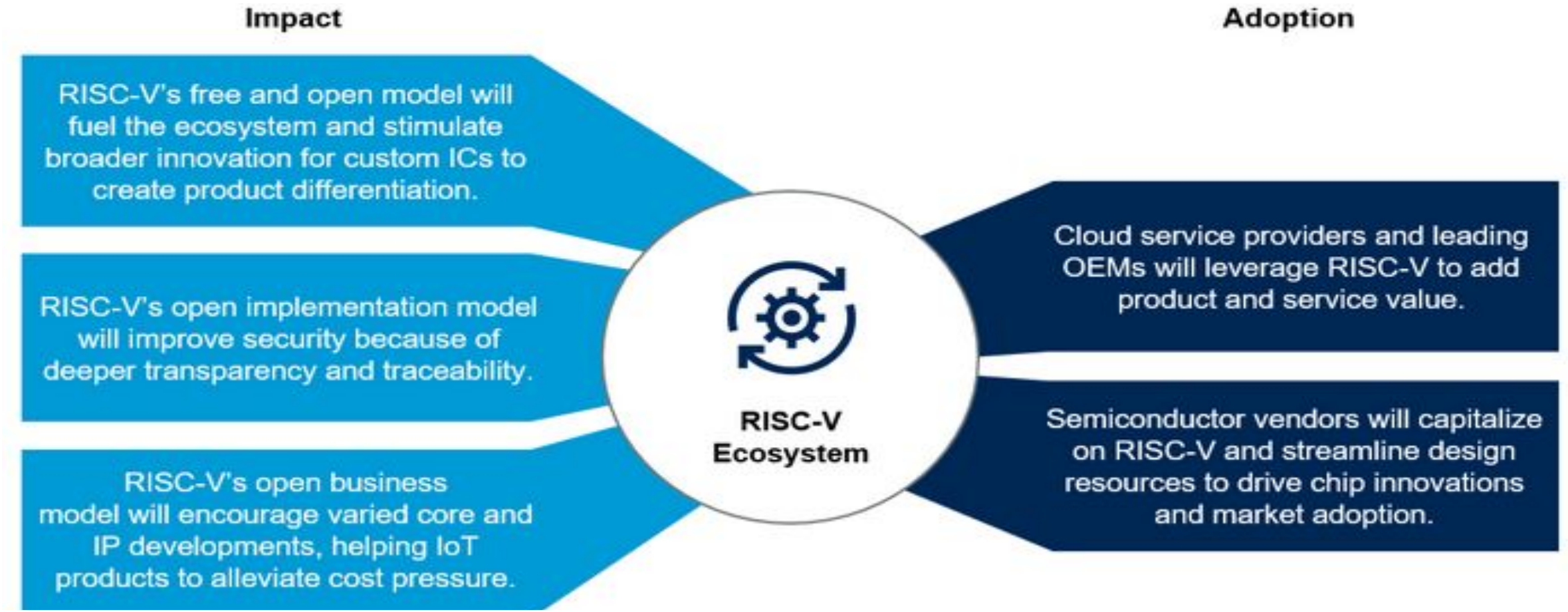
By 2025, 40% of application-specific integrated circuits (ASICs) will be designed by OEMs, up from around 30% today.

Custom ICs Based on RISC-V Will Enable Cost-Effective IoT Product Differentiation

Gartner, June 2020

Source: Gartner

RISC-V's open model will spur adoption by cloud service providers and streamline resources for chip vendors

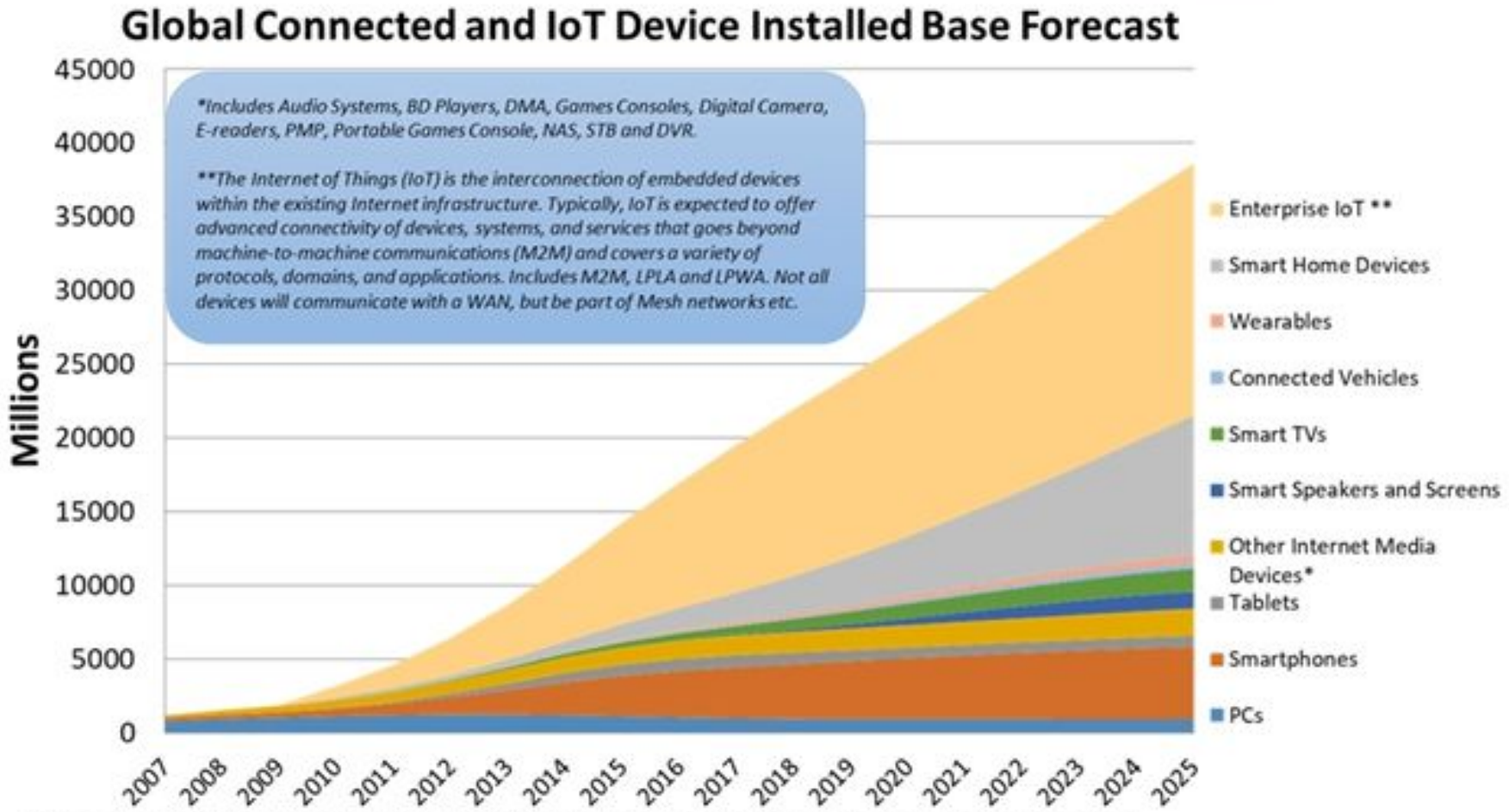


Source: Gartner
ID: 46523_C

50 billion connected and IoT devices

demand security and custom processors by 2030

STRATEGYANALYTICS

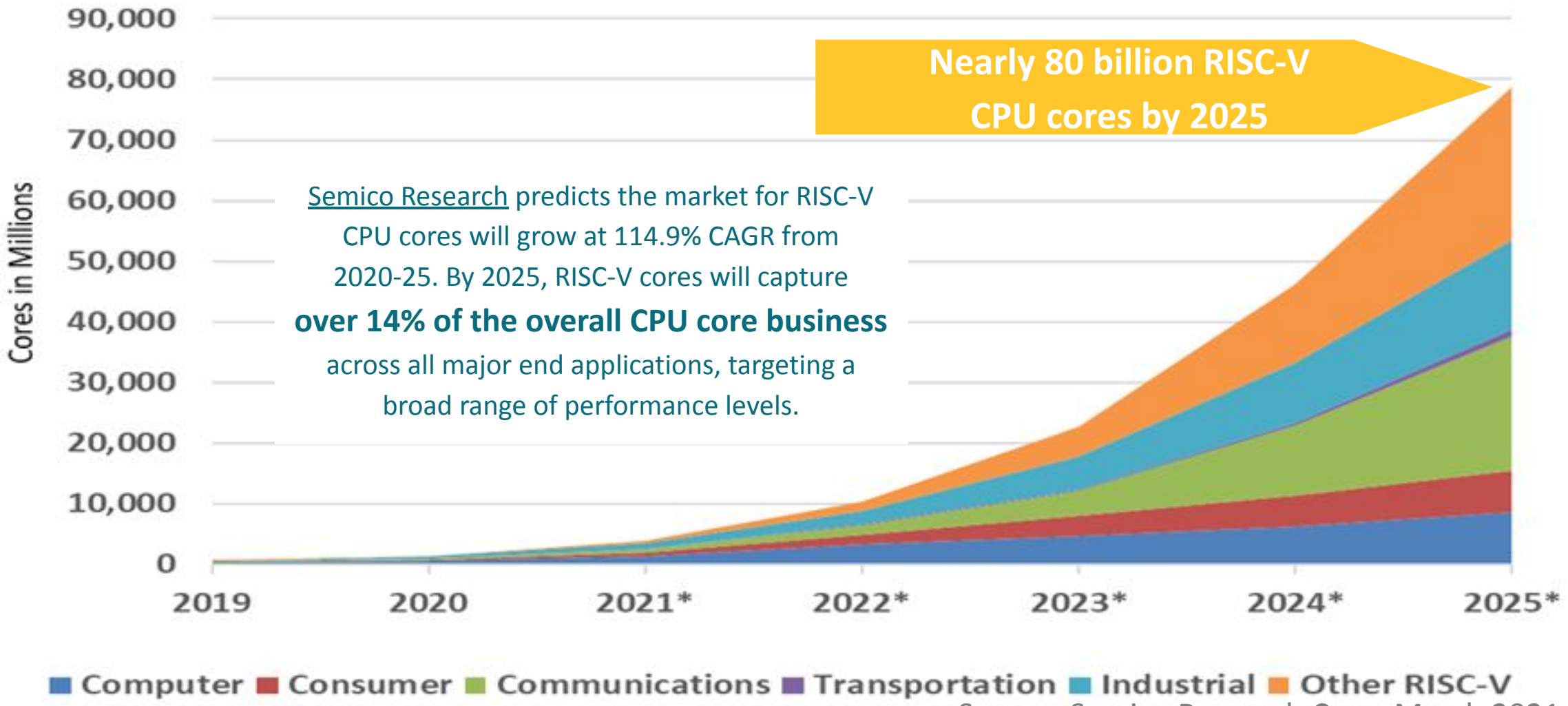


Source – Strategy Analytics research services, May 2019: IoT Strategies, Connected Home Devices, Connected Computing Devices, Wireless Smartphone Strategies, Wearable Device Ecosystem, Smart Home Strategies

RISC-V®

Source: Strategy Analytics

Rapid RISC-V growth led by industrial



Source: Semico Research Corp, March 2021

RISC-V®

RISC-V is the foundation of the Open era of computing

- **4k+ individuals in 60+ RISC-V work groups** and committees
- **330+ RISC-V solutions** online including cores, SoCs, software, tools, and developer boards
- **29 local RISC-V community** groups, with more than **5,400 engineers**
- We're in the news! We have **40k+ followers on social media** and across the last year, we have participated in **135+ news articles** along with amplifying RISC-V community news 450+ times.

RISC-V®

RISC-V Special Interest Group on HPC


RISC-V®
Special Interest Group – High Performance Computing
SIG-HPC
https://lists.riscv.org/g/sig-hpc

SIG-HPC Vision & Mission: RISC-V: IoT to *HPC*

Vision:

The technical and strategic imperatives that guide the RISC-V ecosystem development to enable an Open HPC Ecosystem…

Mission:

…enable RISC-V in a broader set of new software and hardware opportunities in the High Performance Computing space, from the edge to supercomputers, and the software ecosystem required to run legacy and emerging (AI/ML/DL) HPC workloads.

RISC-V®

SIG-HPC: An Open era of HPC!

- CPUs, Accelerators, other hardware units, and coprocessors
- Verification and compliance infrastructure and methodologies specific to HPC
- Alignment and engagement and IP enablement.
- RISC-V software ecosystem alignment
- Engage and represent RISC-V in compute intensive industry and academic events
- Identify key industrial and academic partners.
- Support global technology independence with a RISC-V ecosystem roadmap and partners

RISC-V®

SIG-HPC Initiatives

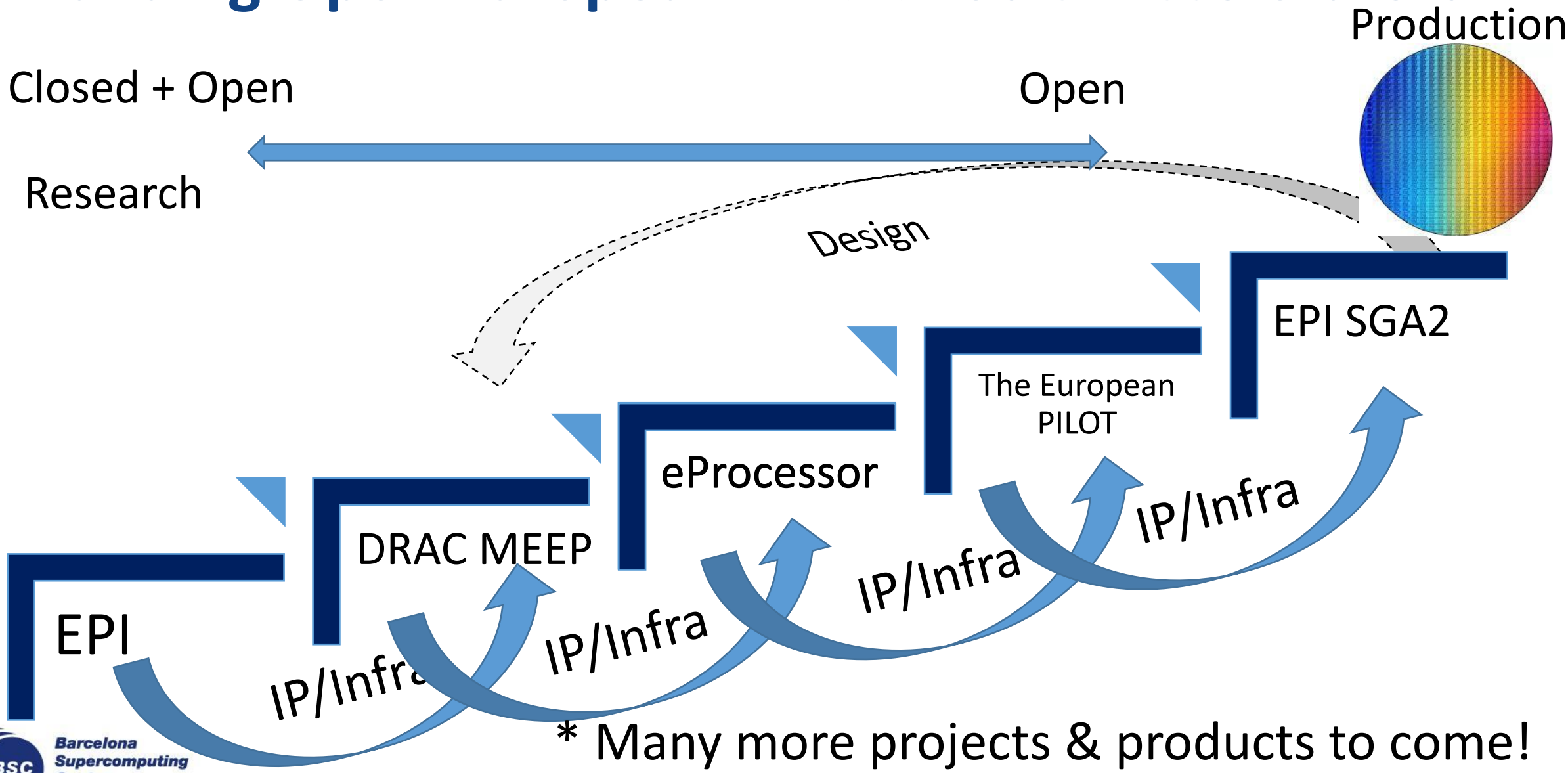
- Guide and enable the community
  - Virtual Memory
    - SV57, SV57K, SV64, SV128
  - **HPC SW & HW ecosystem & roadmap**
  - Accelerators
  - ISA Extensions
  - **HPC Software Stack**
    - Starting with HPC Libraries

You Can Help

- Get involved in SIG HPC
- https://lists.riscv.org/g/sig-hpc
- Subscribe:
  - Send email to: sig-hpc+subscribe@lists.riscv.org
- Monthly meetings
  - 3rd Thursday of the month
  - Next meeting: June 16th @ 16:00 CET

Getting Started

Building Open European HPC CPUs & Accelerators



Coming Soon: SUPERcomputing Risc-V LAB SUPER-V @ BSC

- Enabling the development of the HPC ecosystem for RISC-V based systems
- Variety of systems
  - RISC-V clusters running HPC software stack (i.e., Unmatched cluster)
  - RISC-V Experimental/research platforms for vector architectures
    - FPGA-based system
    - Software emulators
    - Hybrid software/hardware emulators
- HPC Software ecosystem development
- And more…
- Access information coming soon…
  - Easybuild and Gentoo first success story

SUPER-V@ BSC

- Clusters:

Board	OS	Details
PolarFire	Fedora	4 cores w/ 2 GB
BeagleV	Fedora	2 cores w/ 8 GB
Unmatched	Fedora/Ubuntu	4 cores w/ 16 GB
Allwinner D1 (Vector extension)	Fedora	1 core w/ 2 GB

Emulators:

- A RISC-V soft vector core running in an FPGA.
- The Vehave RISC-V emulator on top of QEMU
- The Vehave RISC-V emulator on top of a native RISC-V core

- RISC-V Software Stack:
  - Linux, SLURM
  - Compilers:
    - go/1.17
    - openmpi/fedora/4.1.1_gcc10.3.1
    - llvm/EPI-0.7-development
    - openmpi/ubuntu/4.1.1_gcc10.3.0
    - llvm/EPI-development
    - python/fedora/2.7.16
  - Tools
    - extrae/3.8.3
    - papi/6.0.0
    - perf/5.11.10
    - singularity/3.8.2
  - Libraries
    - boost/1.77.0
    - glibc/fedora/2.33
    - openBLAS/0.3.15
    - fftw/3.3.9_gcc10.3.1_ompi4.1.1
    - libunwind/git
    - openBLAS/0.3.17

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

RISC-V in RESEARCH

- 2019: What is Open Source Hardware??
- 2020: Open Source Hardware
- 2021: RISC-V? Roadmap?
  - November roadmap report
  - Horizon Europe Work Programme 2021-22:
    - Open Source Hardware (OSH) appears 6 times
    - CSA Roadmap
- 2022: Build RISC-V!!!
  - KDT JU Work Programme 2021 v13:
    - **RISC-V appears 25 times**
    - OSH appears 2 times
- **More to come in EuroHPC, KDT, and other calls!**

Doug Norton @Inspire Semiconductor
David Donofrio @ Tactical Computing Labs
Michael Wong @Codeplay

ISC High Performance
The HPC Event.

InspireSemi™

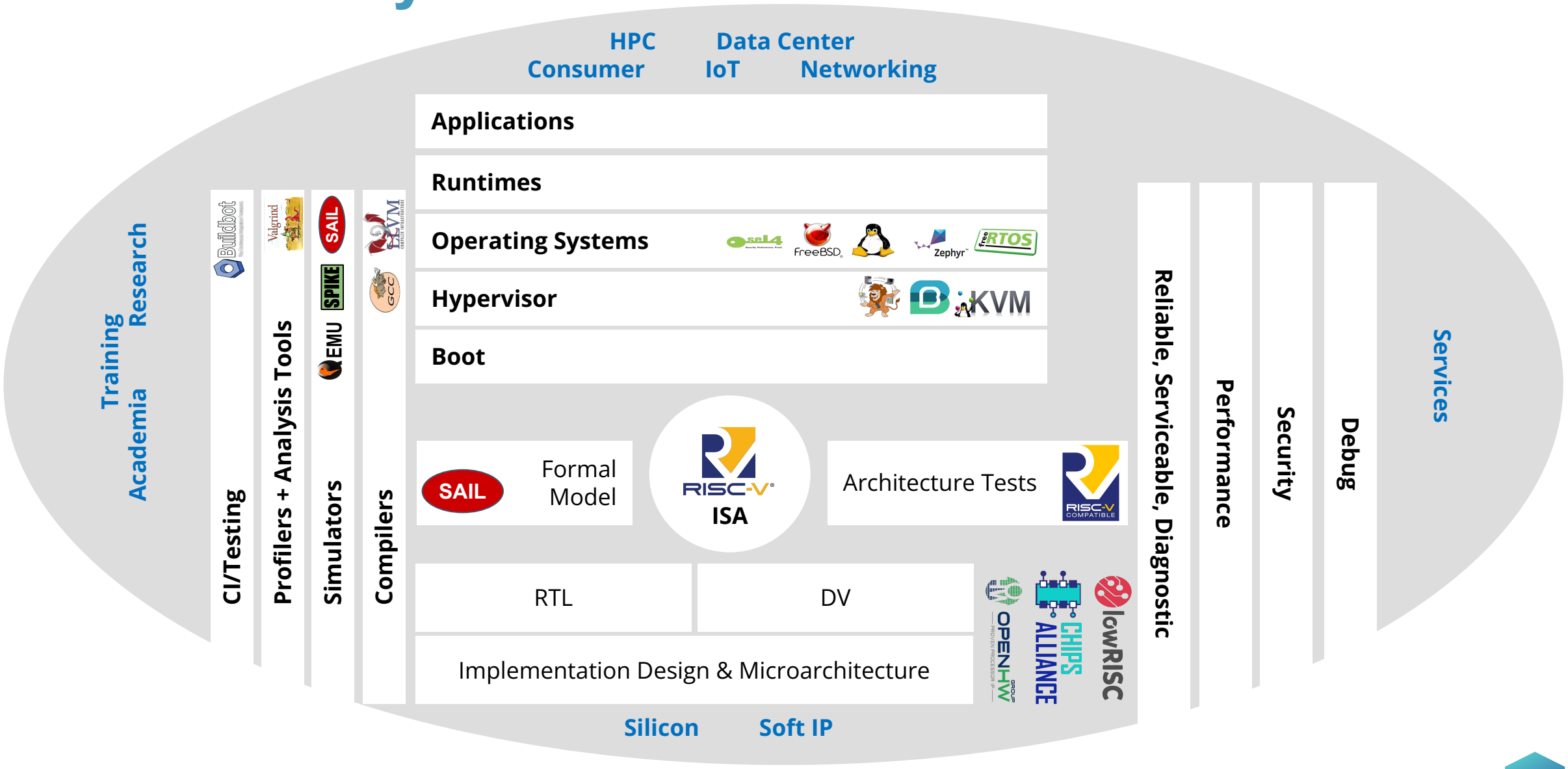
Breakthrough compute performance:
new standards of speed, efficiency, and flexibility

RISC-V®

HPC Ecosystem & Roadmap

Doug Norton

RISC-V Ecosystem



Open Ecosystem HW/SW Co-Design

GROMACS, NAMD, Quantum Espresso, …

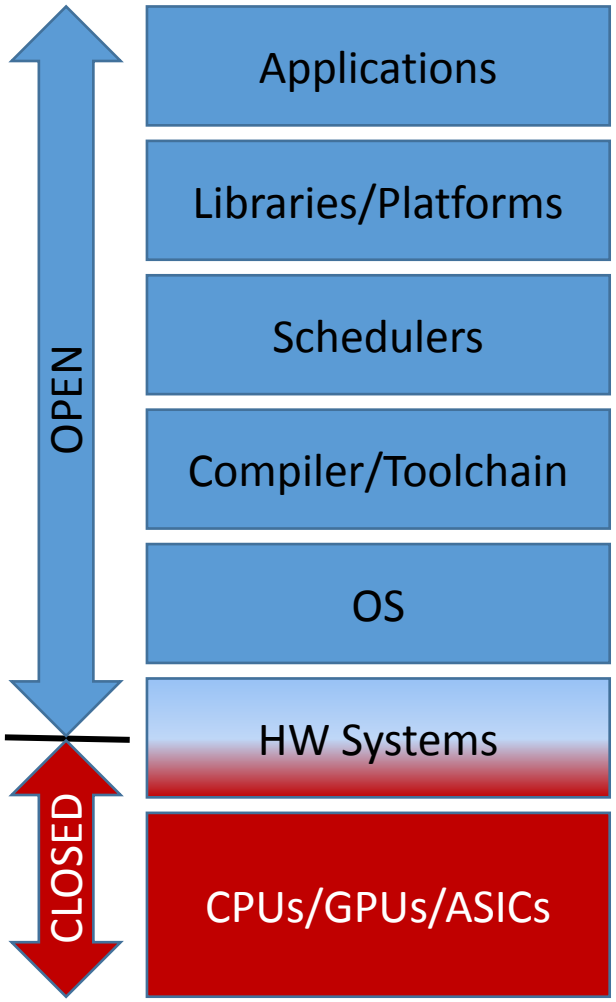
FFTW, BLAS, SLEEF, …

SLURM, xCat, MPICH, OpenMP, …

GCC, LLVM, GDB, Binutils, …

Linux, FreeBSD, …

https://github.com/riscv/riscv-software-list
https://github.com/riscv-test/riscv-hpc



RISC-V HPC Ecosystem

- HPC/AI hardware under development
  - E.g. – SiFive, Andes, Esperanto, InspireSemi, Rivos, Codasip
  - Vector support varies
- Linux Operating Systems: RISC-V in mainstream kernel
  - With caveats, i.e. – need F, D, C extensions to run pre-compiled packages
- Key AI frameworks, compilers, and tools exist for RISC-V
  - TensorFlow Lite, PyTorch
  - Standard GCC, Gfortran, GDB toolchains
  - LLVM RISC-V back-end, MLIR
  - Flang now available and Fortran work underway (F77)
  - Standard HPC libraries (e.g. – BLAS, LAPACK, FFTW)
  - OpenMP, MPI
  - SLURM

RISC-V HPC Ecosystem Roadmap/Gaps

- Hardware
  - More RISC-V HPC hardware needed for software dev, & optimization
  - Will help drive business case for ISVs
- Software
  - Additional Linux support (e.g. – RHEL, SUSE, Rocky)
  - Expand to full TensorFlow support
  - Expand high performance FORTRAN support
    - F90, 2003, 2008, 2018
  - Vector support needs to be resolved
    - Some early hardware implemented 0.7 spec pre-release
    - 1.0 final spec not backward compatible to earlier releases

RISC-V
80% READY FOR HPC

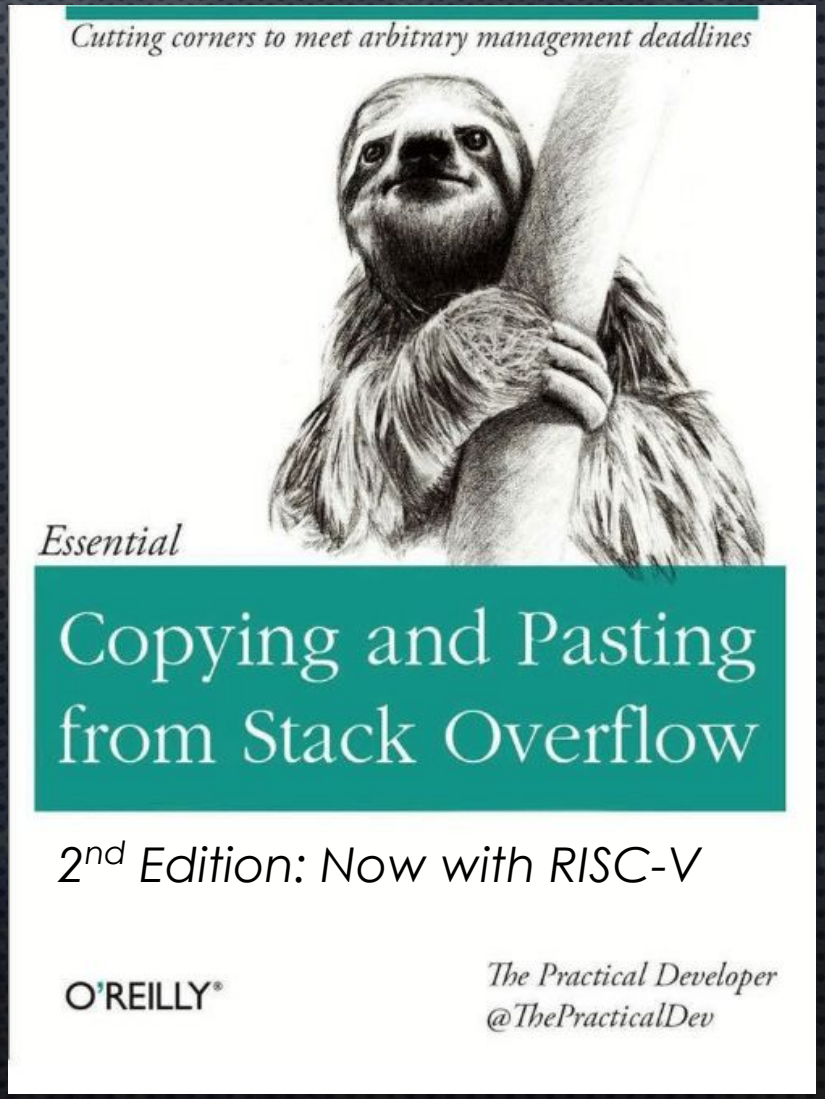
David D. Donofrio, Chief Hardware Architect

John D. Leidel, Chief Scientist

ISC 2022

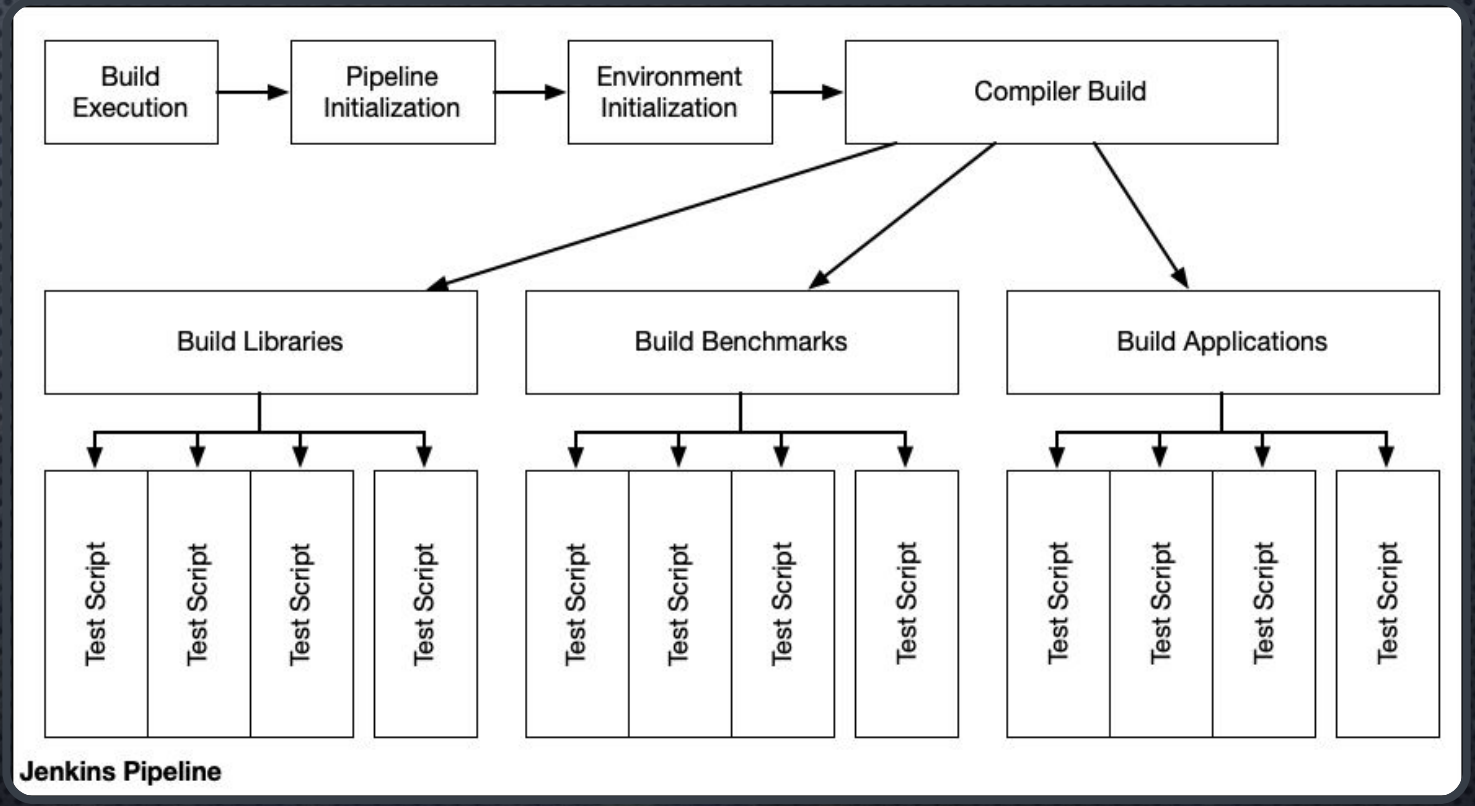
RISC-V HPC ECOSYSTEM

- The RISC-V Community has made enormous progress
  - Production compilers
  - Real OS ports
  - Wide industry adoption
  - Large community for support, development, etc.
  - Vector, bit manipulation, etc. extensions
- Larger diversity in HW architectures has paved the way for RISC-V Adoption
- This is an opportunity for the HPC community to develop and tailor solutions to our requirements
  - xBGAS



TCL CI EFFORTS

- Jenkins-based CI suite for HPC tools
  - Cross compilation flow
- Utilizes different baseline compilers to build:
  - Libraries
  - Benchmark Suites
  - Applications
- Goal: Check for functionality across software stacks, **NOT** performance
- https://riscv-test.org/



✓	⚙	llvm-project-12.0.1	4 days 3 hr - #44
✗	☁	llvm-project-master	18 days - #97
✓	⚙	riscv-gnu-toolchain-master	4 days 3 hr - #98

HPC LIBRARY PORTING EXAMPLE – OPENUCX

- HPC Libraries often stress the boundaries of HW and SW
  - Many elements of things typical devs are "insulated" from
- OpenUCX includes self-modifying code
  - X86, ARM, PPC already supported
- Porting to RISC-V exposed subtle ISA differences
  - Example: How to efficiently deal with 32-bit immediates?
- The porting of libraries of runtimes will require a concentrated effort
  - No fundamental restrictions on RISC-V
  - Creation of an HPC Platform Specification?

David Donofrio, Chief Hardware Architect

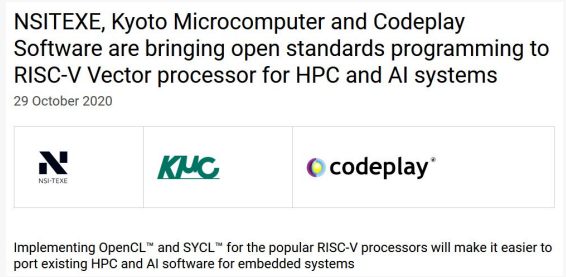
John D. Leidel, Chief Scientist

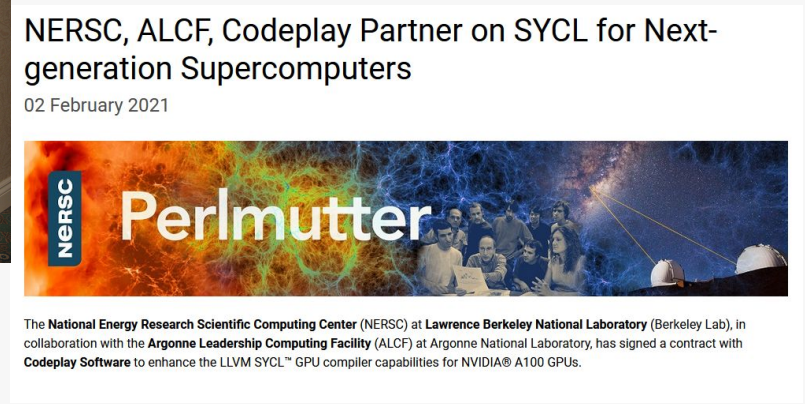
{ddonofrio,jleidel}@tactcomplabs.com

Distinguished Engineer

Michael Wong

- Chair of SYCL Heterogeneous Programming Language
- RISC-V Datacenter/Cloud Computing SIG Chair
- ISO C++ Directions Group past Chair
- Past CEO OpenMP
- ISOCPP.org Director, VP
  http://isocpp.org/wiki/faq/wg21#michael-wong
- michael@codeplay.com
- fraggamuffin@gmail.com
- Head of Delegation for C++ Standard for Canada
- Chair of Programming Languages for Standards Council of Canada
  Chair of WG21 SG19 Machine Learning
  Chair of WG21 SG14 Games Dev/Low Latency/Financial Trading/Embedded
- Editor: C++ SG5 Transactional Memory Technical Specification
- Editor: C++ SG1 Concurrency Technical Specification
- MISRA C++ and AUTOSAR
- Chair of Standards Council Canada TC22/SC32 Electrical and electronic components (SOTIF)
- Chair of UL4600 Object Tracking
- http://wongmichael.com/about
- C++11 book in Chinese:
  https://www.amazon.cn/dp/B00ETOV2OQ





We build GPU compilers for some of the most powerful supercomputers in the world

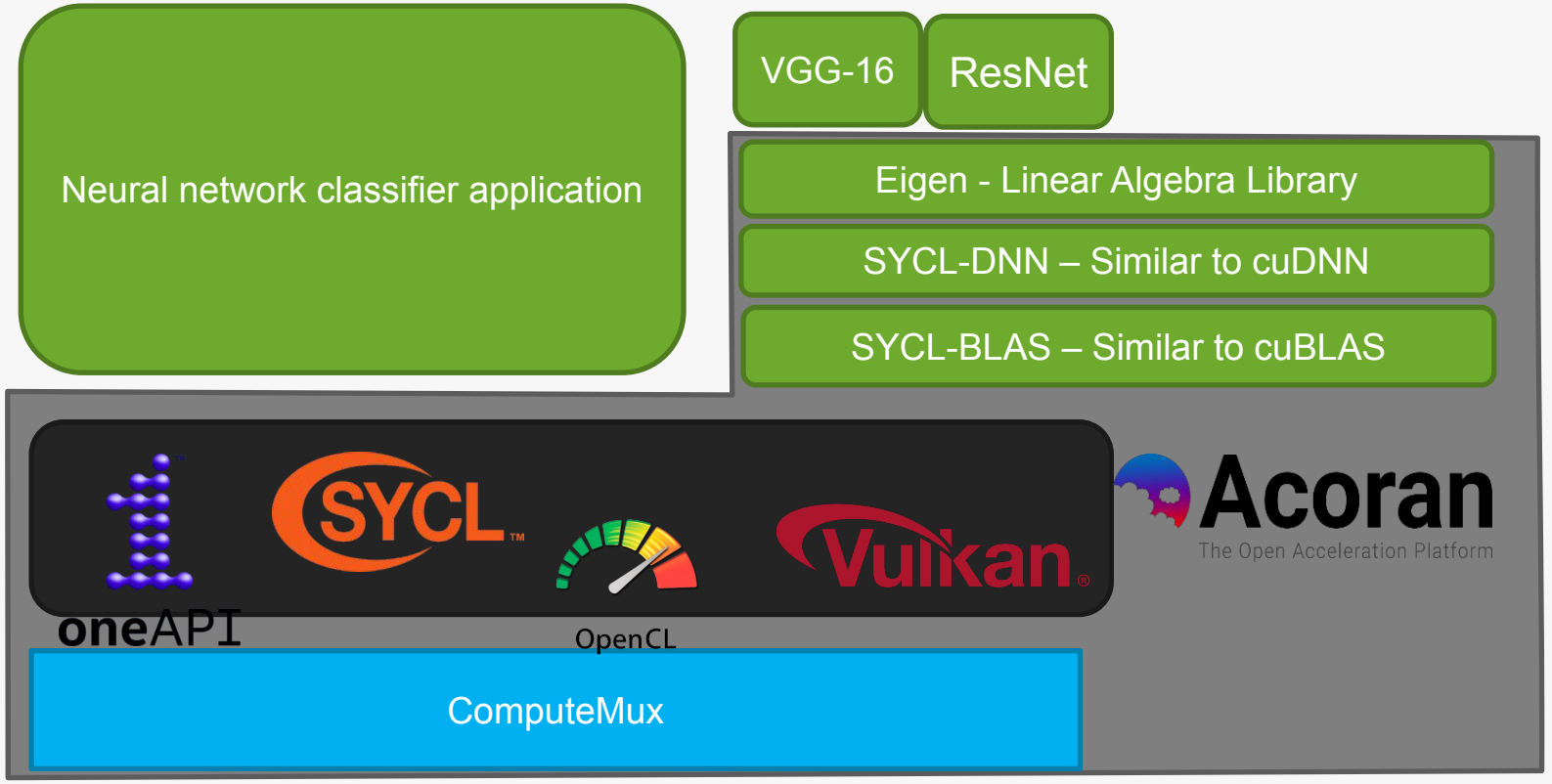
SYCL on RISC-V Architecture

C++ software

Compiler

Driver interface API

RISC-V hardware



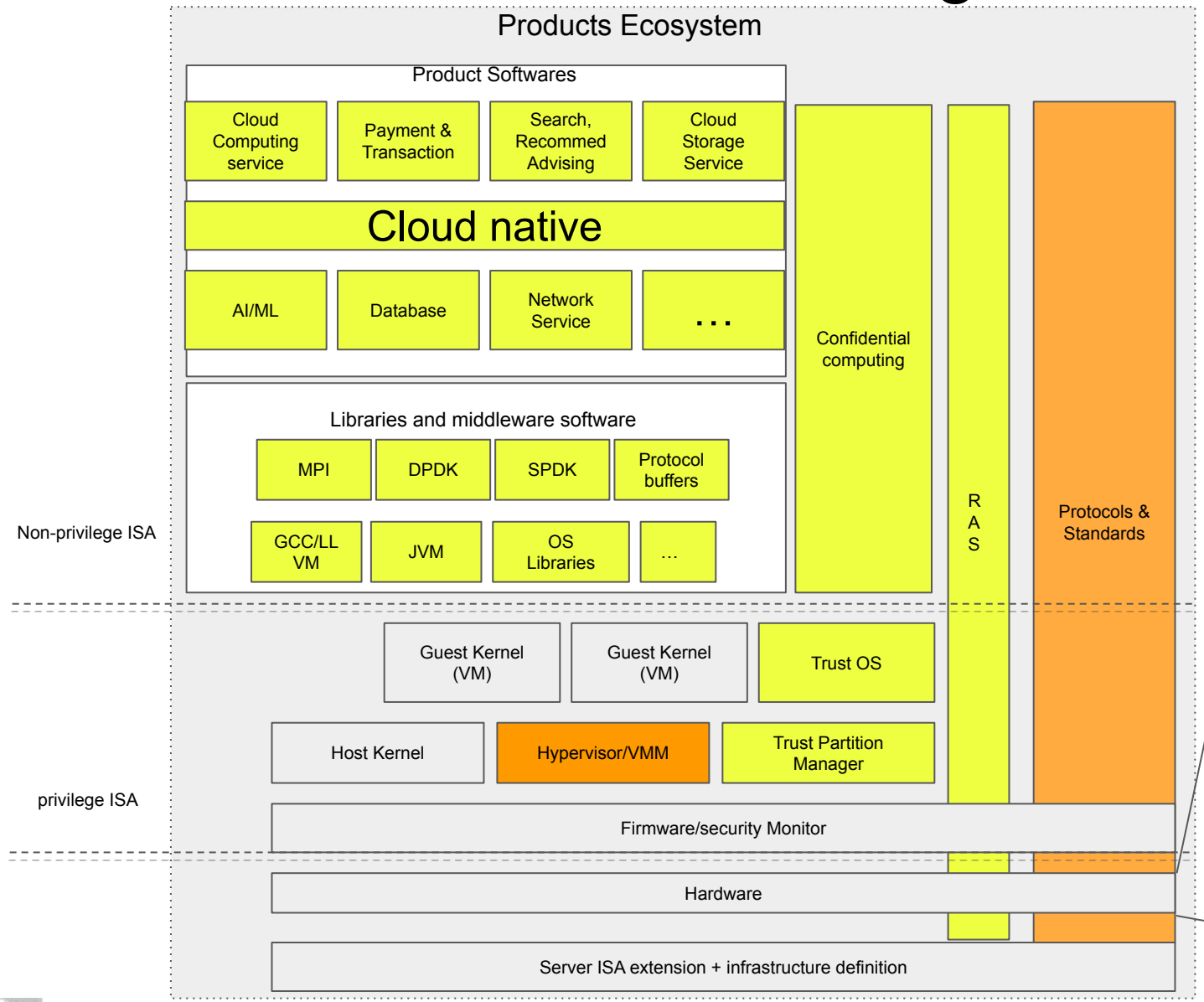
The Acoran platform provides all the supporting open source libraries and frameworks needed to build this neural network demonstration

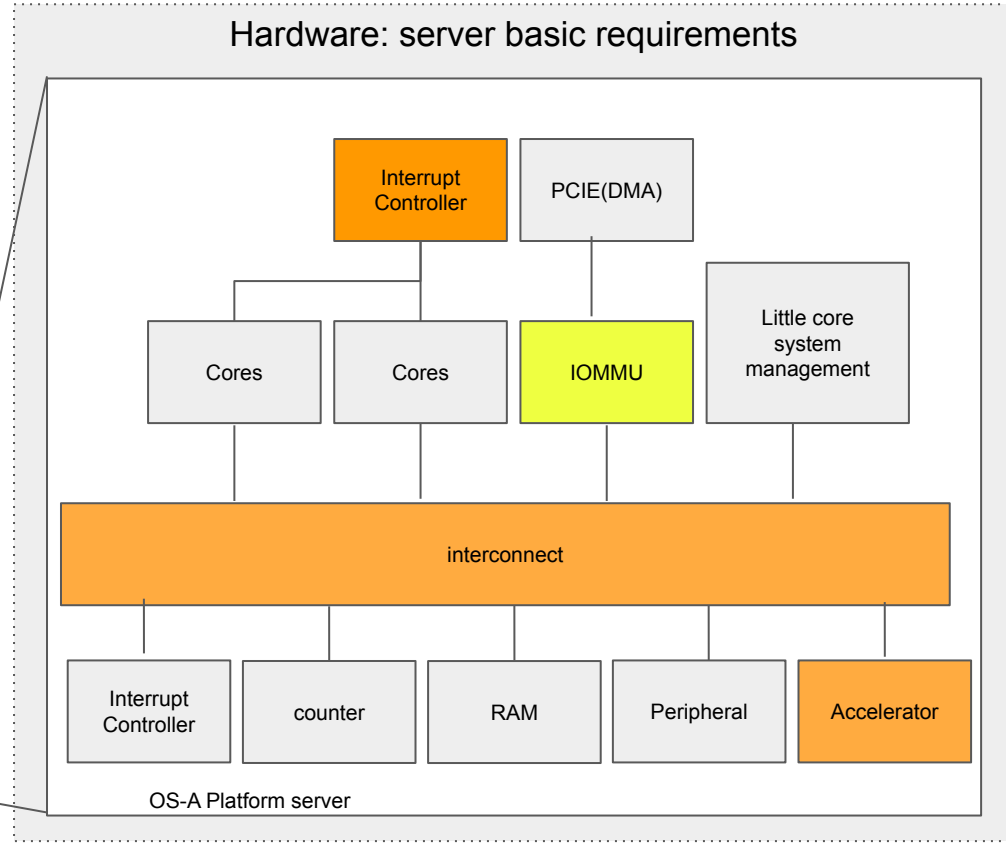
Road to success block diagram

ISA and software partial ready, minor improvement required

Ecosystem needed, no ratified spec

Lack of a stable version definition, need definition or improvement





Thank you

john.davis@bsc.es