Barcelona Supercomputing Center
Centro Nacional de Supercomputación

EXCELENCIA SEVERO OCHOA

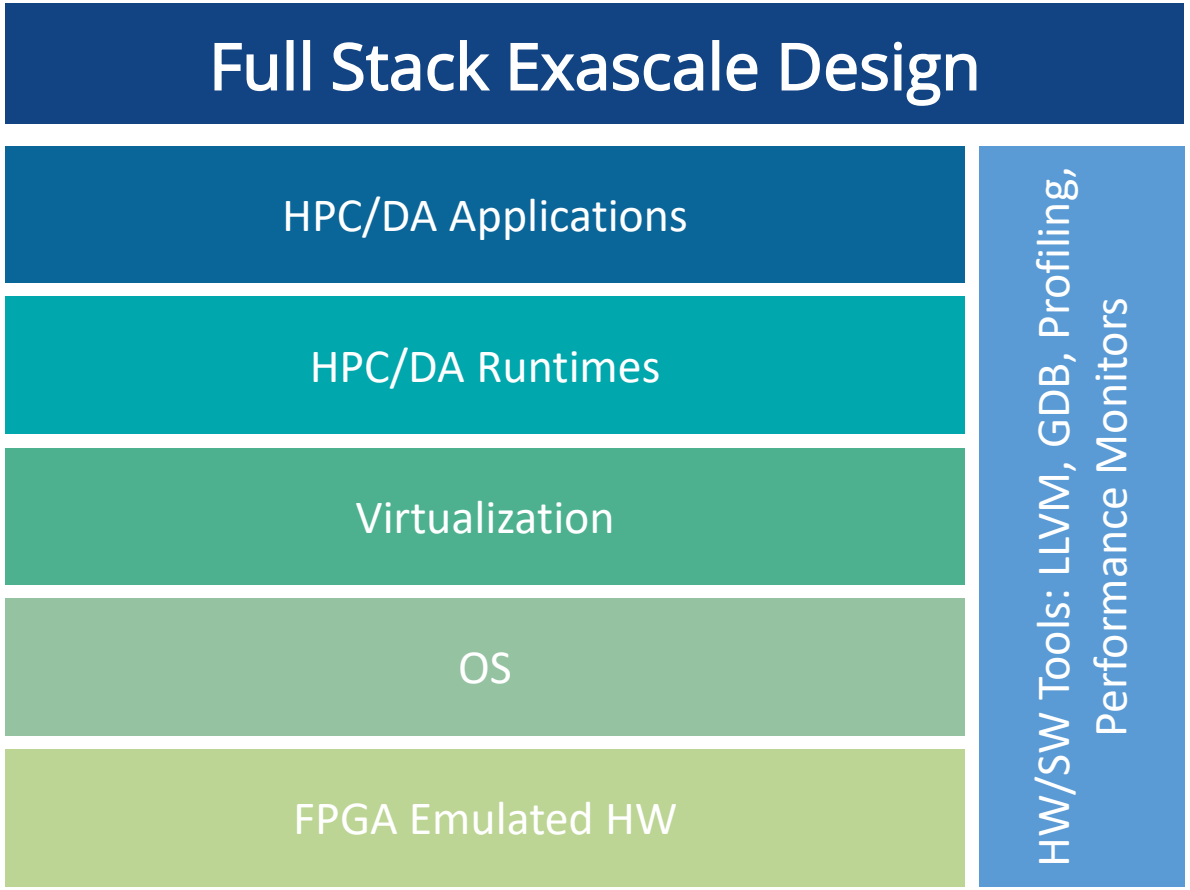
MEEP

MareNostrum Experimental Exascale Platform

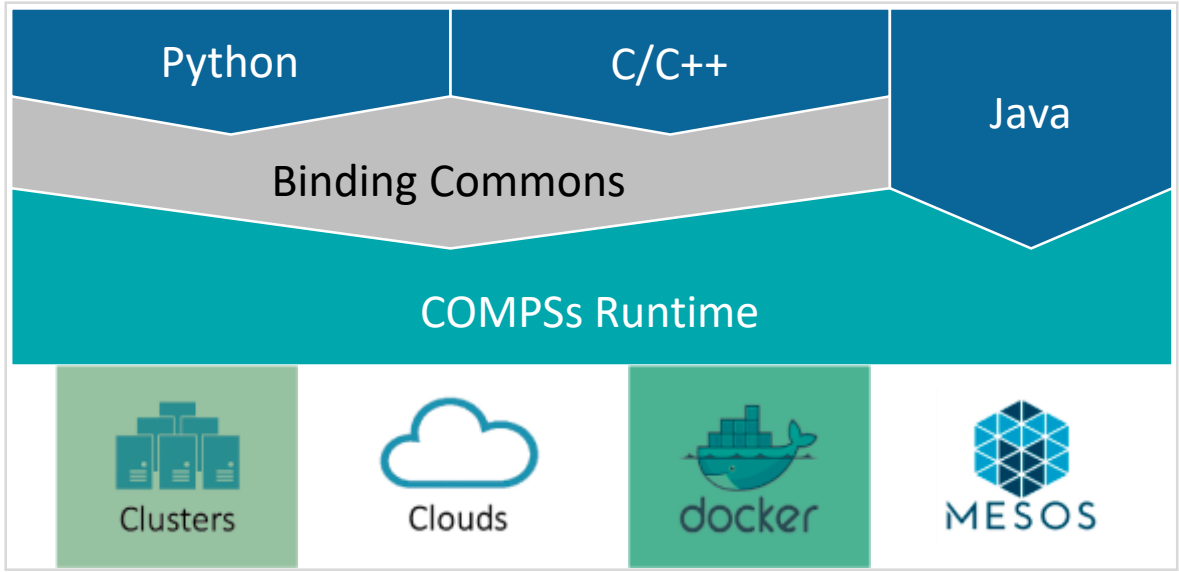
Name

Position

MEEP Full Stack



MEEP SW Stack



Performance Optimisation and Productivity

OmpSs-2 Programming Model

OpenMP

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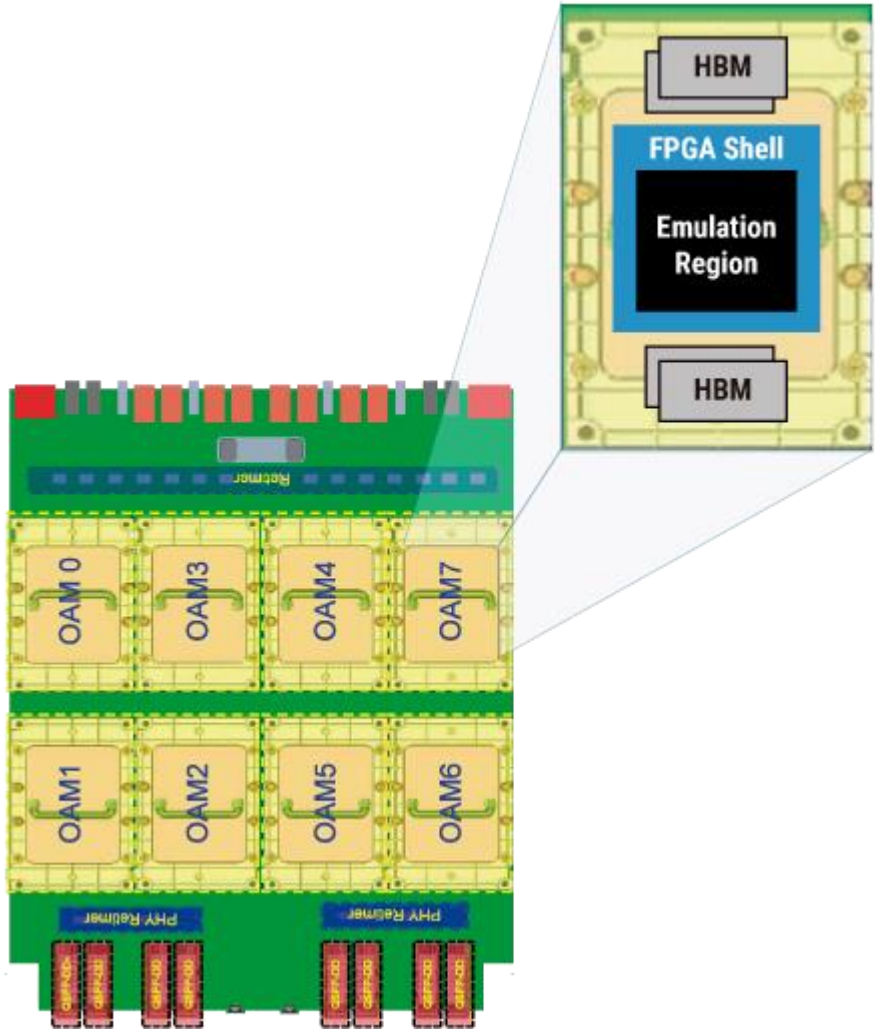
MEEP HW Stack

FPGA Shell:

· External Interfaces: I/O, DRAM, etc.

Emulation Region:

· Cores: Scalar, vector, etc.
· Accelerators: Tensor, NN, etc.
· Caches and other memory structures



MEEP Benefits

Large-scale Emulations for Exascale Systems

FPGA Emulation Platform
- OAM FPGA + HBM
  - RISC-V: Scalar+DLP accelerators+Memory

Software stack development vehicle
- Apps down to OS

Improve Technology Readiness Level (TRL):
- RISC-V: Scalar + Vector (and other DLP accelerator) cores
- Memory hierarchy
- Software stack

Thank you

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