MEEP

MareNostrum Experimental Exascale Platform

https://meep-project.eu/

Starting Date: 1 January 2020 | End Date: 31 December 2022

Partners

Motivation

MEEP is a flexible FPGA-based emulation platform that will explore hardware/software co-designs for Exascale Supercomputers and other hardware targets, based on European-developed IP. The project provides two functions:

- An evaluation platform of pre-silicon IP and ideas, at speed and scale.
- A software development and experimentation platform to enable software readiness for new hardware.

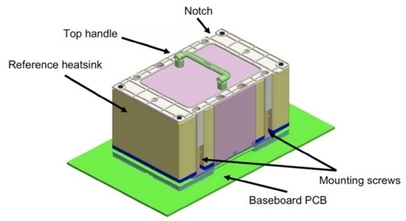
MEEP will enable software development, accelerating software maturity, compared to the limitations of software simulation. IP can be tested and validated before moving to silicon, saving time and money.

MEEP: Infrastructure to Build Future Exascale Systems

Approach

MEEP is a performance evaluation and software development vehicle for future silicon chip designs. The project's objectives are:

- Define the FPGA-based platform and align with state-of-art OEM/ODM roadmaps.
- Then, the platform will be acquired and set up with a single node used as a target for system software and hardware development.
- Finally, this will be followed by a multi-accelerator on multi-mode demonstration, if possible, MEEP will also demonstrate multiple accelerators on a single node.



*MEEP: FPGA building block for a single emulated accelerator**

** This system can be a testbed for other accelerators ranging from tightly-to loosely-coupled systems*.

Objectives

- Define, develop, and deploy an FPGA-based emulation platform targeting European-based Exascale Supercomputer RISC-V-based IP development, especially hardware/software co-design.
- Develop a base FPGA shell that provides memory and I/O connectivity to the host CPU and other FPGAs.
- Build FPGA tools and support to map enhanced EPI and MEEP IP into the FPGA core, validating and demonstrating European IP.
- Develop the software toolchain (compiler, debugger, profiler, OS, and drivers) for RISC-V based accelerators to enable application development and porting.

Vision

- MEEP will create a state-of-the-art emulation and software development platform for Exascale systems based on European technology.
- It will support the development of new and reusable IP targeting FPGAs and eventually, ASICs. The novelty of the accelerator is a so-called self-hosting accelerator.
- MEEP will be of a size and scale that goes far beyond normal academic or industrial prototyping platforms, enabling chip and system emulation. It needs to be of sufficient scale, as proposed, to emulate a meaningful fraction of the HPC environment.

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