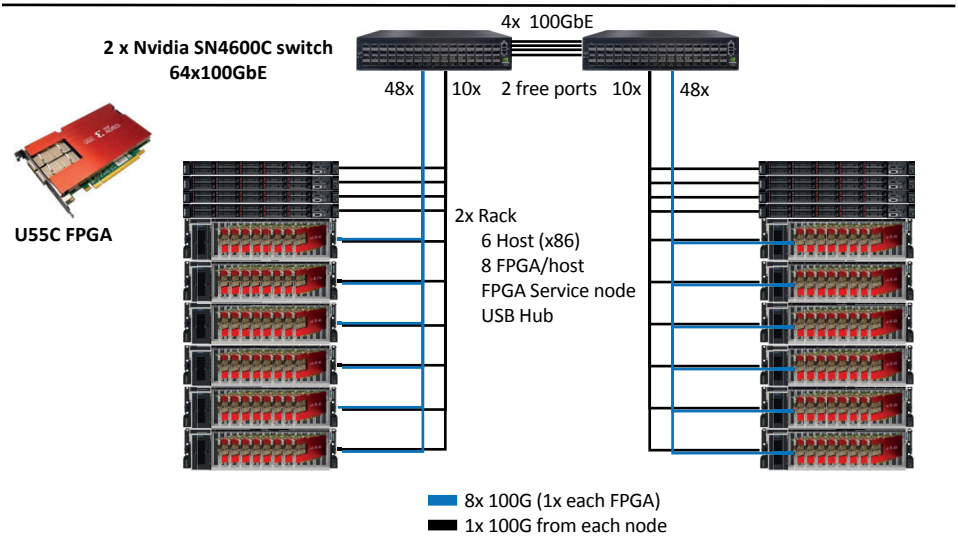
MEEP

MareNostrum Experimental Exascale Platform

MEEP an FPGA-based digital lab for exploring hardware/software co-design for Exascale Supercomputers, which provides:

- An evaluation platform of pre-silicon IP and ideas
- A software development vehicle to enable software readiness for new hardware

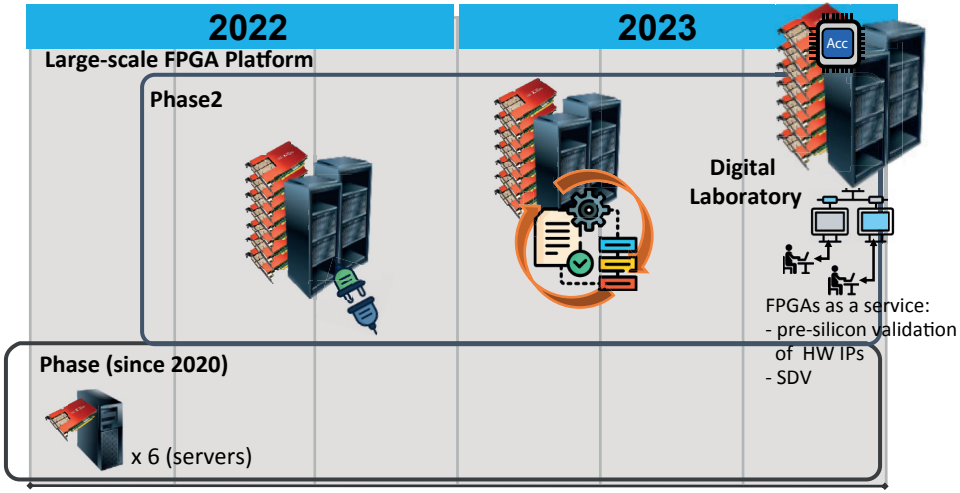
MEEP platform characterization



Goals

- Accelerate Hardware Design Process of European HPC IP (accelerators, CPUs, etc.)
- Accelerate and enable Software Development for new HPC hardware designs
- Reduce development time and costs

MEEP platform Roadmap



Motivation

- End of Moore's Law and power constraints require software/hardware co-design
- Chip fabrication increasing in cost, need to validate pre-silicon designs
- Leverage the technology scaling in mobile chips leads to a chiplet architecture for HPC
- Hardware platform that can be used for software development

The MEEP project has received funding from the European High-Performance Computing Joint Undertaking (JU) under grant agreement No 946002. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Spain, Croatia, Turkey.

www.meep-project.eu