



RISC-V Labs

Contributing to the RISC-V HPC Ecosystem

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A Quick **RISC-V** Overview



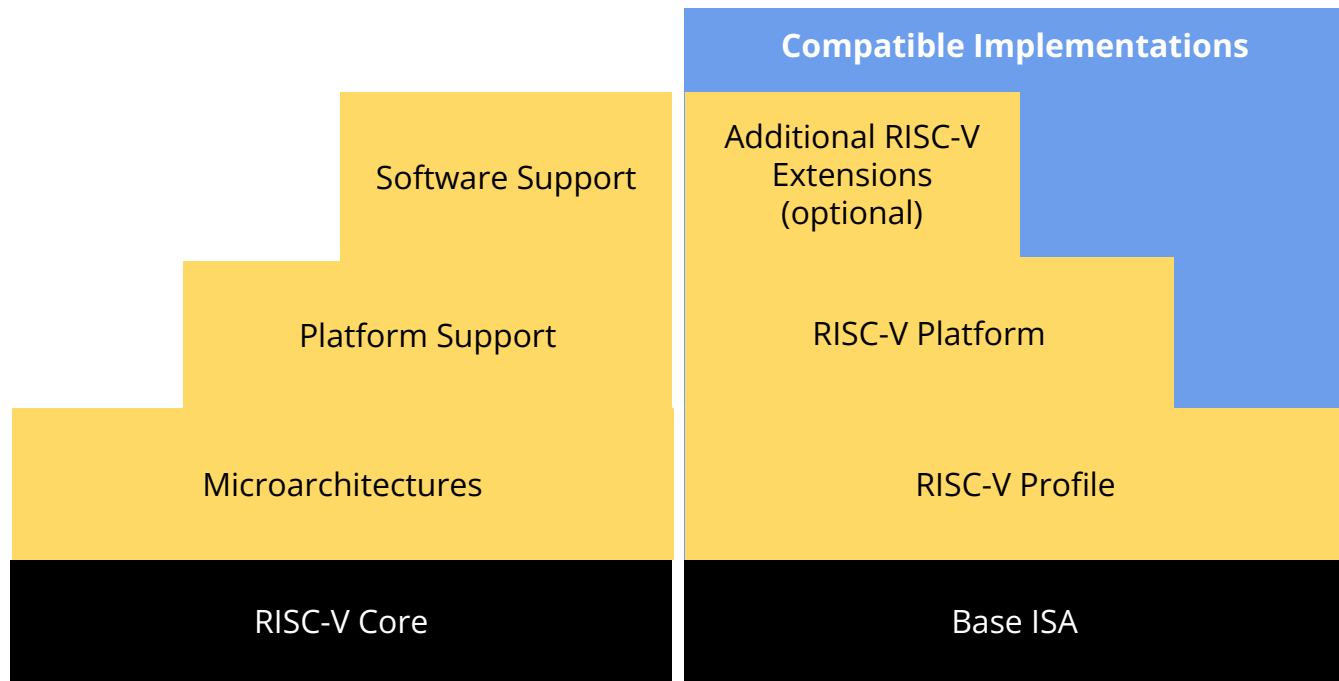
Who is RISC-V

RISC-V International is a global nonprofit association based in Switzerland. Founded in 2015, RISC-V brings together **3k+ members** in more than **70 countries** across industries and technical disciplines.

RISC-V supports the open RISC-V instruction set architecture, developing additional extensions, tools, and resources paving the way for the next 50 years of computing design and innovation. RISC-V also connects the community and industry through academia, commercialization, and strategic leadership.

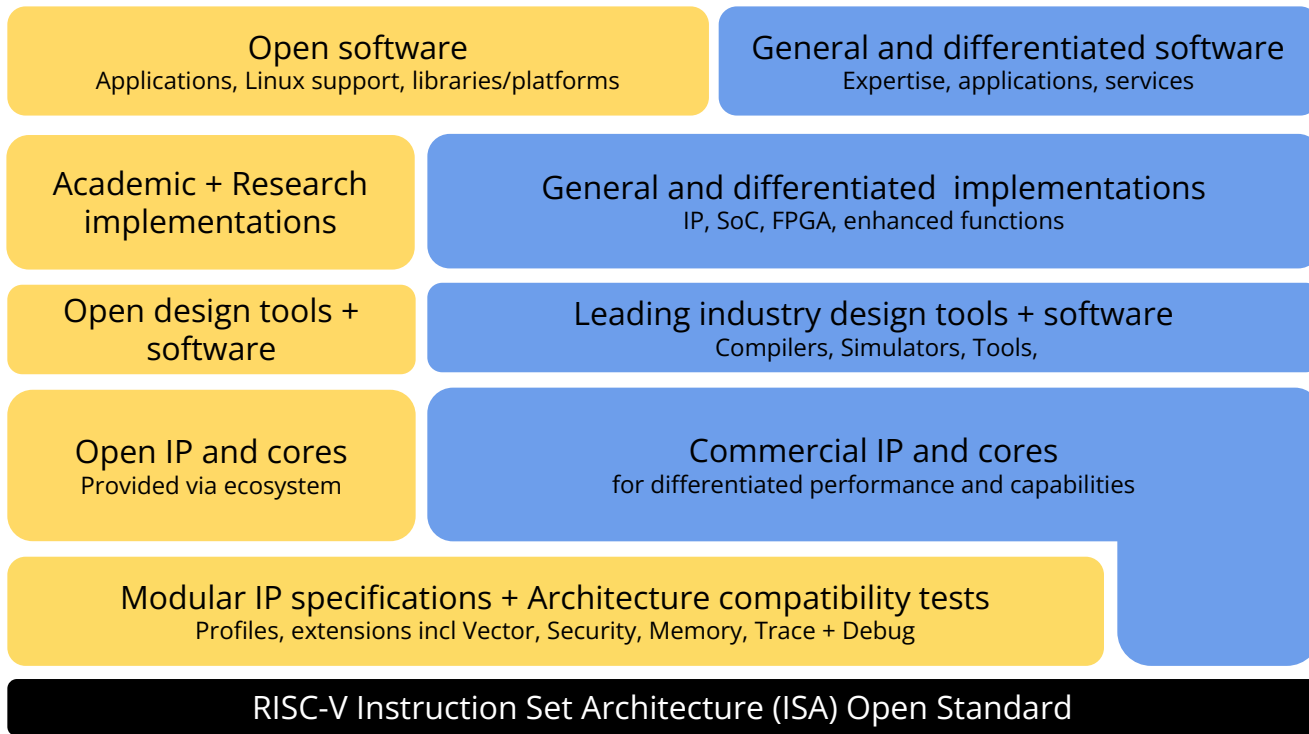


Building Hardware using RISC-V



Standardization, Modularity, and Flexibility

Open standard IP specifications for modular designs based on decades of investment and expertise



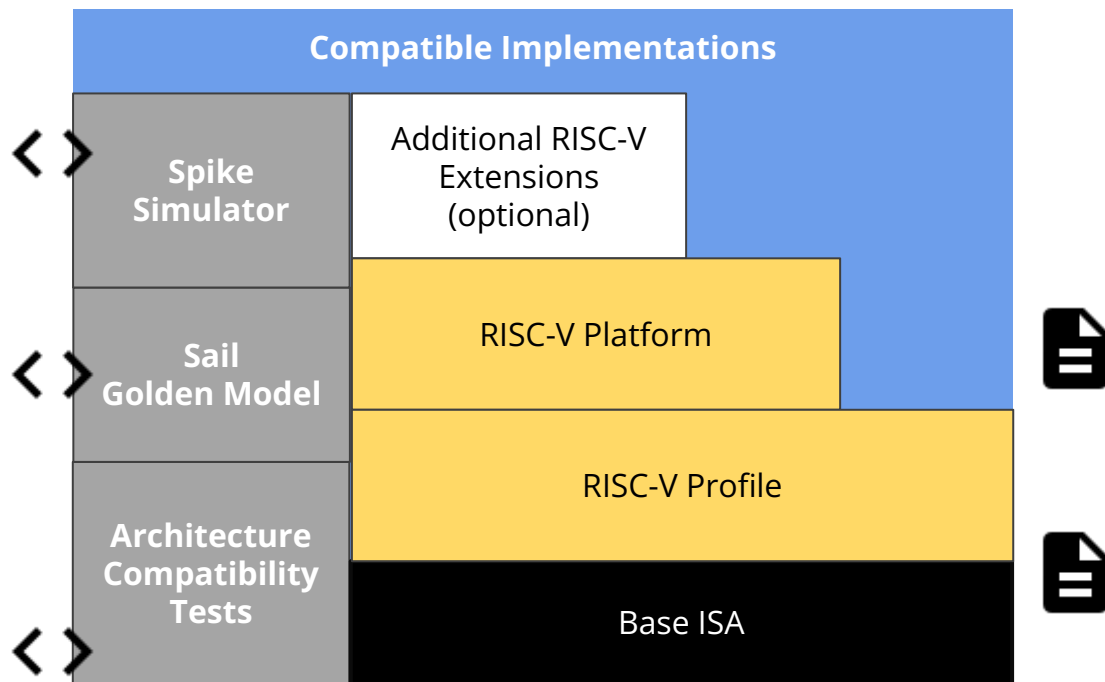
Commercial innovation and differentiation to solve full spectrum of compute challenges

Hardware Compatibility using RISC-V

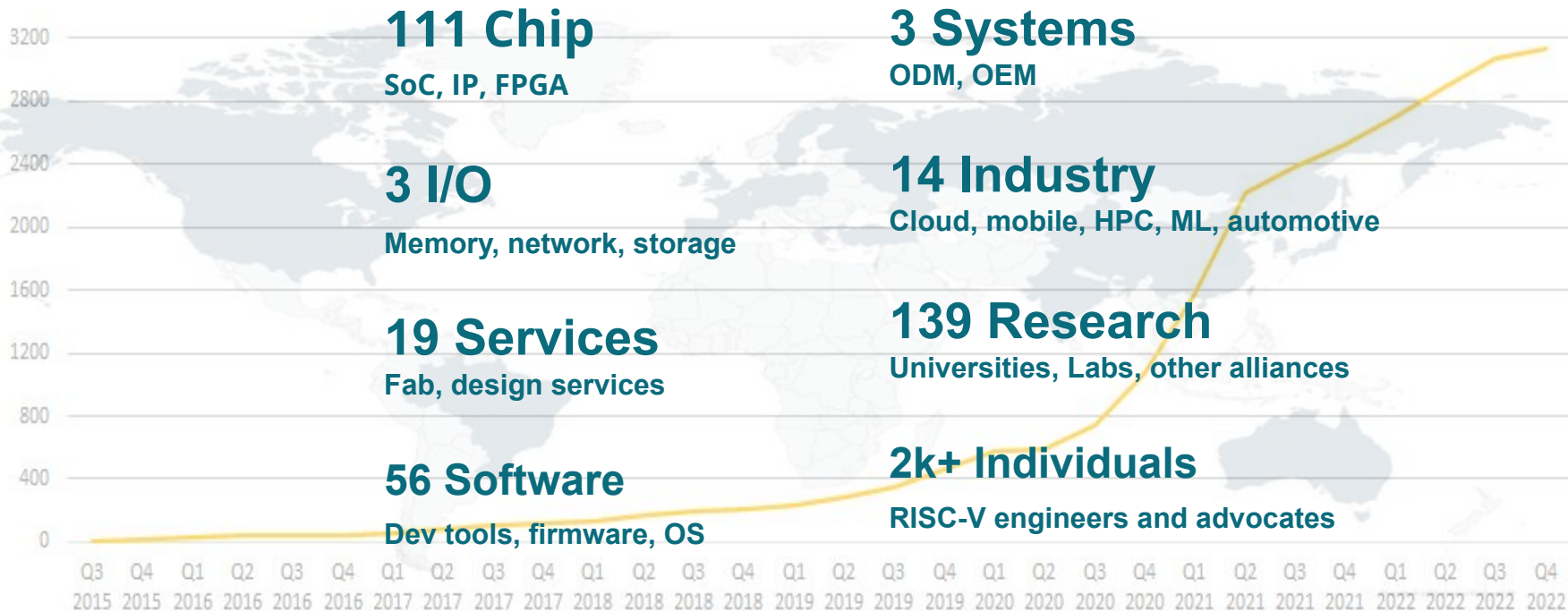
- › Profiles
- › Platforms
- › Sail Golden Model
- › Architecture Tests
- › Spike Simulator

 = Specification Document

 = Open Source Code



More than 3,100 RISC-V Members across 70 Countries



Oct 2022

RISC-V Technical Community



- **GitHub**
<https://github.com/riscv>*
- **Mailing Lists**
<https://lists.riscv.org>
- **RISC-V Wiki**
<https://wiki.riscv.org>



Development Partners
Developer Boards
RISC-V Labs



RISC-V Development Partners Overview

- Streamline collaboration
- Advance projects critical to extension ratification
- Foster RISC-V understanding through mentorship
- Publicly recognize contributions

<https://riscv.org/risc-v-development-partner/>

RISC-V Development Partners Commitment

- Maintain their membership in RISC-V International
- Align with RISC-V Leadership
- Provide PoC Examples
- Minimum Contribution Goals

RISC-V Commitment to DevPartners

- Leadership Support & Mentorship
- Project Planning Oversight
- Public Recognition
- Additional Support (hardware, software, etc)

RISC-V Development Partners



中国科学院
CHINESE ACADEMY OF SCIENCES



ISCAS

RIOS



10x
ENGINEERS

****Newest Member****

Program Details

- RISC-V Mailing List: dev-partners@lists.riscv.org
- Meetings every 2-weeks, standing time:
 - 2 PM UTC
 - 9 AM U.S. Eastern Standard Time
 - 10 PM China Time
 - 7:30 PM India Time
- First meeting of 2023 on January 17
 - See [tech.meeting](#) calendar for all meetings

How to Become a DevPartner

1. Join the DevPartners community (see previous slide)
2. Start attending the DevPartners meetings (see previous slide)
3. Review the criteria in the [DevPartners policy](#)
 - a. Complete a Proof-of-concept (on-boarding) project with a mentor
 - b. Commit to supporting a minimum of 3 medium sized projects simultaneously
 - c. Provide a DevPartner liason to work with RISC-V Team
4. Reach out to help@riscv.org with any questions



Development Partners
Developer Boards
RISC-V Labs



RISC-V Developer Boards Program Overview

- Enable OS Support
- Enable Upstream OSS Support
- Build Educational Resources
- Embrace Emerging Technologies
- Foster good-will (Do Well by Doing Good)

RISC-V Developer Boards Web Pages

Main landing page (“Catch the traffic”)

<https://riscv.org/risc-v-developer-boards/>

Program Details (“Run the business”)

<https://riscv.org/risc-v-developer-boards/details/>

RISC-V Developer Boards

Program Overview

The RISC-V Developer Boards program serves to evangelize and promote the RISC-V architecture by partnering with RISC-V hardware vendors to donate hardware to projects to:

- Drive success of RISC-V member products and services, to enable operating system distributions support,
- Grow upstream open-source software community adoption,
- Build educational resources,
- Embrace emerging technologies which use the RISC-V architecture, and
- Foster software ecosystem engagement and good-will.

Participant projects will submit a plan of usage and be required to document their results using the board. In addition, RISC-V vendor members are running their own programs and coordinating with RISC-V International.

Want to help? Want a free board? Visit our details page to submit a proposal for a project!

Vendor members contributing and offering boards:

ALLWINNER antmicro ALIBABA CLOUD beagleboard.org MICROCHIP RIOS SiFive StarFive 赛昉科技

Program Details

To participate in the program, submit a project proposal. Great proposals:

- Have clear impact – contributing patches, testing, or documentation – to a significant, established upstream community
- Are proposed by proven open-source software contributors who provide a link to their documented track record in GitHub, GitLab, etc.
- Impact strategic RISC-V products and markets
- Conform to the footprints of current or near immediate DevBoard hardware
- Come from RISC-V members who are active in our communities

While not all of these attributes are requirements, the more qualities a project has, the greater the chance of it being accepted. Additionally, programs will run independently, with no project carry-over. So, bookmark our page and submit your proposals with each new platform that meets your requirements.

How To Apply

1. Review the terms (blue box on the right)
2. Select an active program (below) which best meets our requirements
3. Apply using the form link provided in the Status section of the program

If you have any questions, reach out to dev-boards@riscv.org.

If you'd like to join the program planning, join the [RISC-V Developer Board Program](#) community.

If you are a RISC-V member and have a board for the program, complete our [RISC-V Developer Boards Partnership Form](#) to start the ball rolling.

Active Programs

The following programs are currently being run. You may apply to multiple programs but please apply only to the programs where the hardware meets your needs.

Board Name	Details	Status
ICE-V from QWERTY Embedded Design 60mm x 32mm, ESP32-C3H4 SOC, 400 KB SRAM, 384 KB ROM, Lattice iCE40 FPGA (2K LUTs), Wi-Fi, Bluetooth, 1-USB, GPIO for serial, ADC, or I2C	info	Open. Closes November 15, 2022. Expect product buy in late 2022. Apply
VisionV2 from Starfive Pico-ITX, 4-LUT4 cores, 8 GB memory, 2-USB 2.0, 2x USB 3.0, 1-1 Gb Ethernet, 1-10/100 Mb Ethernet, 1 M.2 key for NvMe stack, 40-pin GPIO	info	Open. Closes December 15, 2022. Expect product buy in early 2023. Apply
ROMA laptop from DeepComputing and Xiallyte Laptop, 4- XuanTu C310 processor @ 2.5 GHz, 16 GB memory, 256 GB SSD	info	Open. Closes December 15, 2022. Expect very limited product buy in early 2023. Only strong projects should apply. Apply
VisionV1 from Starfive Pico-ITX, 2-LUT4 cores, 8 GB memory, 2-USB 2.0, 2-USB 3.0, Wi-Fi, 1-Gb Ethernet, 40-pin GPIO	info	Closed. Board purchase started.

How to Engage

- If you're interested in either collaborating with RISC-V on a DevBoard program or you want to help guide the various board programs:
 - a. Join the [RISC-V Development Board Program](#) (Google Group)
 - b. Attend the most time-convenient month meeting ([meeting discussion](#))
 - c. Complete a [Partner proposal form](#) for you program
- If you'd like a developer board so that you can contribute to the ecosystem:
 - a. Review the active programs on the DevBoards [Program Details](#) page
 - b. Propose a project using the **Apply** button for applicable board(s)

Program Process

- Program management
 - Public mailing list, open membership: [RISC-V Development Board Program](#) (Google Group)
 - 2 meetings per month, alternating East-friendly, West-friendly
- Individual board programs:
 - Conceived or proposed ([Partner proposal form](#))
 - Program posted to “Details” webpage, with cut-off date for proposals
 - Developers apply through board-specific form created, e.g. [VisionFive V2](#)
 - Projects selected based on proposal
 - Boards purchased and shipped with no cost to developers
 - Projects added to the RISC-V Developer Board Community
 - All boards have a summary post with documentation and links

Program Process - continued

- Good projects proposals:
 - Have clear impact – contributing patches, testing, or documentation – to a significant, established upstream community
 - Are proposed by proven open-source software contributors who provide a link to their documented track record in GitHub, GitLab, etc.
 - Impact strategic RISC-V products and markets
 - Conform to the footprints of current or near immediate DevBoard hardware
 - Come from RISC-V members who are active in our communities

Note: Not all attributes are required, but more is better!

- Project requirements (give back):
 - Monthly and Final status
 - Willing to work with RISC-V marketing to document project and results

Sample Developer Board Community Email

Welcome to the new VisionFive Board Projects

May 6, 2022 ([link](#))

<snip>

Those you are not familiar with the board, can learn more here: [VisionFive Single Board Computer Quick Start Guide | RVspace](#)

To those who are newly added to the community, it serves as my communication vehicle with all projects in the DevBoard Seed program and should be your starting point for getting started and finding help when stuck elsewhere. As new members, you will have the benefits of two additional programs before you -- one for the D1 Nezha board and one for the Unmatched board. The people on this list are passionate about RISC-V and eager to help. So, please reach out as needed.

To get started with your StarFive, VisionFive boards, you'll find the board information anchored at [rvspace.org](#) which included the following 3 user documents:

- [Quick Start Guide](#) - the "Getting Started" section has information about both flashing the SD card but also logging into the pre-configured Fedora image
- [Software Technical Reference Manual](#) - provides details about building components of the platform software stack -- SBI, u-boot, kernel, ...
- [GPIO Header User Guide](#) - details the technical aspects of the attaching peripherals through the GPIO header

Additionally, VisionFive has started an English forum for their board at <https://forum.rvspace.org/c/visionfive/6>. This should be your first stopping place for any problems you encounter while getting started with your board. (Note: you do have to create an account to participate.)

To my knowledge, I have not found any distro-specific pages yet for the VisionFive board, but here are the generic pages for RISC-V which may be helpful:

- Debian for RISC-V: <https://wiki.debian.org/RISC-V>
- Fedora for RISC-V (Unmatched not supported yet): <https://fedoraproject.org/wiki/Architectures/RISC-V>
- openSUSE for RISC-V (Unmatched not supported yet): <https://en.opensuse.org/openSUSE:RISC-V>
- FreeBSD on RISC-V: <https://wiki.freebsd.org/riscv>
- OpenBSD on RISC-V: <https://www.openbsd.org/riscv64.html>
- Zephyr on RISC-V: <https://docs.zephyrproject.org/latest/boards/riscv/index.html>

Note: that this hardware is quite close to the old BeagleV board and thus some legacy documentation may exist.

As you find other links which you think might be helpful, please post them so that others can benefit.

As you hit roadblocks, have questions, or just want to leverage the wisdom of the community, please reach out with questions. We are here to help.

Board Programs

1. Allwinner D1(60 Boards): Complete
 - 36 Academic, 3 Distro, 25 Ecosystem
2. SiFive Unmatched (25 Boards): Complete
 - 6 Academic, 12 Distro, 7 Ecosystem
3. VisionFive V1 (105 Boards): Complete
 - 17 Academic, 38 Distro, 43 Ecosystem, 7 Available
4. ICE-V (20 Boards): Open until 11/15
 - 20 Available
5. Xcalibyte/Deep Computing (10 Laptops): Open until 11/15
 - Awaiting product

Board Programs - Continued

6. VisionFive V2 (TBD Boards): Open until 12/15
 - o TBD

DevBoard Impacts

Note: The projects, institutions, and communities named here are working on RISC-V projects. Being listed does **does not** mean that RISC-V is supported or endorsed by said entity.

Operating Systems

- Debian
- Fedora
- openSUSE
- Ubuntu
- ArchLinux
- Rocky Linux
- Alpine Linux
- FreeBSD
- OpenBSD
- Yocto
- NixOS
- FreeRTOS
- Zephyr
- Sel4
- Plan 9
- Apache Mynewt
- Android
- FlorenceOS

Academic-projects

- Hochschule München University
- NTNU (Norway U. of Science & Tech)
- University of Auckland
- Lanzhou University
- Nanjing University of Posts & Telecom
- Chongqing University
- Nanjing Univ. of Info., Sci. & Tech.
- Hangzhou Dianzi University
- Barcelona Supercomputing Center
- Universidade de Brasilia
- Instituto Politécnico Nacional
- University of California, Berkeley
- Reed College
- Jülich
- IEEC Institute of Space Sciences
- University of Bologna

Communities-enablement

- oreboot
- gcc
- buildroot
- tcpdump
- rust-embedded
- OpenWRT
- Linux kernel
- TinyML
- OPTEE
- SystemTAP
- gdb
- Rust
- LLVM
- MEEP
- FMM
- Ftrace
- openCV
- eBPF
- XDP
- openQA
- U-boot
- Eclipse IoT: UPM, mraa
- RustSBI
- kernelCI, LAVA

DevBoard Program Highlights



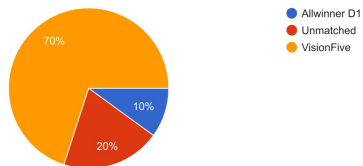
DevBoard Seed Program Feedback

Monthly results

Final results

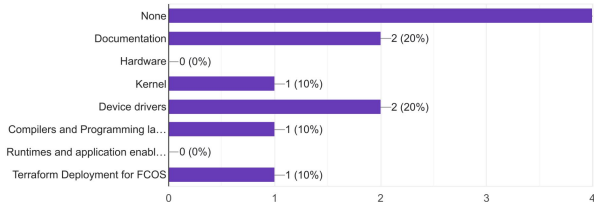
Developer Board

10 responses



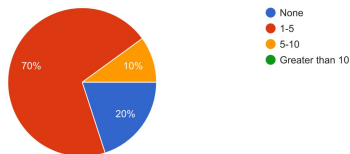
This period I have encountered blockers in the following areas:

10 responses



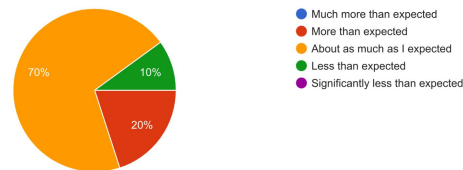
This period I used the board to contribute upstream (code, documentation, or tests) how many times?

10 responses



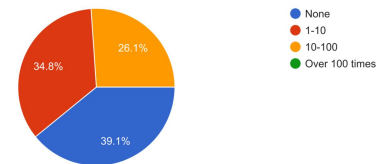
Since my last status report I have accomplished:

10 responses



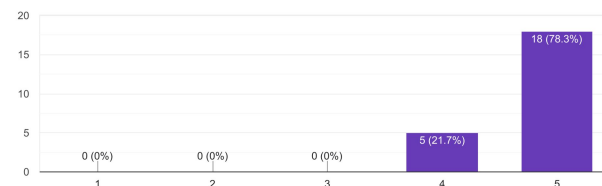
During my project, I used the board to contribute upstream (code, documentation, or tests) approximately how many times?

23 responses



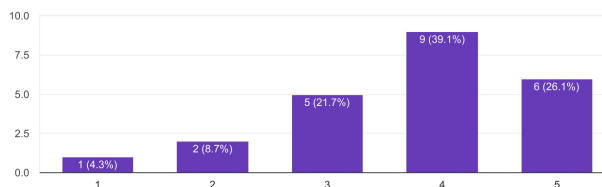
How satisfied were you with the RISC-V Developer Board Program?

23 responses



How satisfied were you with the developer board itself?

23 responses



Program to-date: 187 boards

- Boards to academic projects: 59
- Boards to distro communities: 53
- Boards to ecosystem projects: 75

- Community contributions remained steady - over 60% for 3rd consecutive month.
- Recent Ubuntu support of D1 and VisionFive generated positive feedback.
- Open projects: VisionFive V2, ROMA, ICE-V
- Delayed projects: Polarfire

Development Partners
Developer Boards
RISC-V Labs



RISC-V Labs Program Overview

- Find software regressions early
- Engage open source communities
- Broaden the set of RISC-V platforms available
- Test RISC-V hardware earlier and more broadly
- Connect RISC-V Labs with early hardware access
- Increasing RISC-V recognition and public-relations

**This group is a work-in-progress, working to define the policy and best practices of a new RISC-V program.*

Program Details

- RISC-V Mailing List: lab-partners@lists.riscv.org
- Meetings every 2-weeks, standing time:
 - 3 PM UTC
 - 10 AM U.S. Eastern Standard Time
 - 11 PM China Time
 - 8:30 PM India Time
- First meeting of 2023 on January 17
 - See [tech.meeting](#) calendar for all meetings

How to Become a RISC-V Lab

1. Join the Labs community (see previous slide)
2. Start attending the Labs meetings (see previous slide)
3. Review the criteria in the [draft RISC-V Labs policy](#)
 - a. Minimum of 10 boards or 20 cores (partner provided)
 - b. Provide either CI testing or Sandboxes
 - c. Build a web-presence describing any services, including “in-take” process and usage policies
 - d. Participate in Labs meeting and provide status of testing or service
 - e. Contribute to Labs Best Practices
4. Reach out to help@riscv.org with any questions

Community Resources (future “Labs”)



Sandboxes (boards and containers):

<https://github.com/plctlab/riscv-lab-access>

CI: <https://ci.rvperf.org/>

Patch tracking: <https://patchwork.plctlab.org/>



**Barcelona
Supercomputing
Center**

Centro Nacional de Supercomputación

Sandboxes (boards, simulation, emulation):

<https://repo.hca.bsc.es/gitlab/epi-public/risc-v-vect-or-simulation-environment/-/wikis/HCA-RISC%E2%80%90clusters-user-guide>



Sandboxes (boards, softcores):

<https://riscv.epcc.ed.ac.uk/>

CI: <https://riscv-test.org/>

Doc: <https://www.10xengineers.ai/>

CI: <https://cloud-v.co/>



****Early stages****

Ways to Engage

1. Join the Lab Partner community
 - RISC-V Portal Community: lab-partners@lists.riscv.org
2. Become a Lab Partner
 - CI testing
 - CI service
 - Sandbox service
3. Utilize Labs resources to grow the RISC-V software ecosystem
 - Get resources (previous page)
 - Port your favorite applications

Thank You!

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